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EDN®

VOICE OF THE ENGINEER

ISSUE 17
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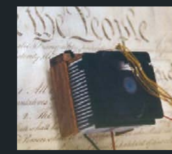

WHO ARE YOU BUYING YOUR EDA SOFTWARE FROM?

DON'T GET HOOKED ON PIRATED SOFTWARE

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VME FOSTERS A FABRIC FUTURE

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VNAs AND TDRs: TAKING THE MEASURE OF THE NEW MILLENNIUM

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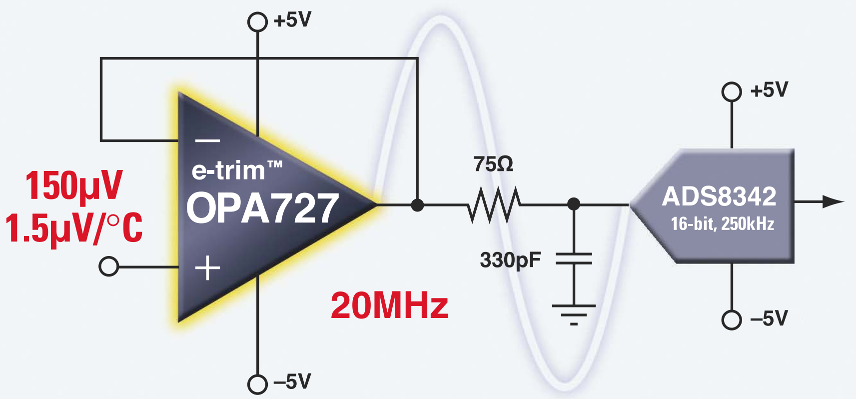
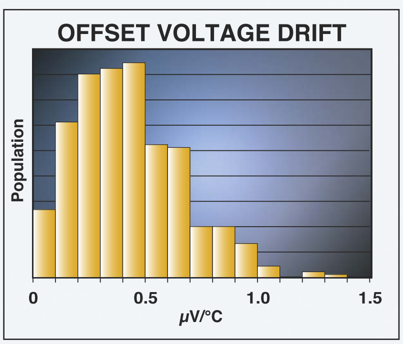
POWER GOES DIGITAL

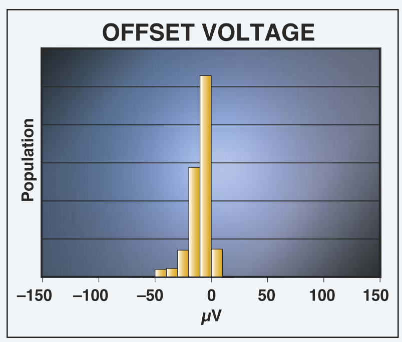
Page 75

150µV max Offset, 20MHz Bandwidth

New e-trim™ Technology Offers 1.5µV/°C max Drift







Using the new **e-trim™ technology**, the OPA727 amplifiers are **calibrated** not only for offset voltage, but also for the variation of **offset voltage over temperature** — a **feature offered only by TI**.

Device	V_{OS} (µV) (max)	Drift (µV/°C) (max)	Band-width (MHz)	Slew Rate (V/µs)	Supply Voltage (V)	I_Q (mA/ch)	Smallest Package	Price Starts 1K
OPA727/28	150	1.5	20	30	4-12	4.3	DFN 3x3mm	$1.45
OPA725/26	3000	4 typ.	20	30	4-12	4.3	SOT23	$0.90

Burr-Brown Products from Texas Instruments

▶ e-trim™ Technology

- Post-packaging digital trimming
- Trimming of offset drift for best-in-class temperature stability
- Very tight offset distribution

▶ Features

- 150µV max V_{OS} offset
- 1.5V/°C max drift
- Low input current: 10pA
- Wide bandwidth: 20MHz
- Rail-to-rail output
- Wide supply range: 4V to 12V, ±2V to ±6V
- Micropackages

MSOP-8 DFN, 3x3mm

▶ Applications

- Precision ADC driver
- Photodiode amplifier
- Active filters
- Medical scanners
- Security scanners
- High-end audio
- Fluid analyzers

Amplifier Selection Guide
Datasheets and Samples

www.ti.com/opa727 ◦ 800.477.8924, ext. 11999

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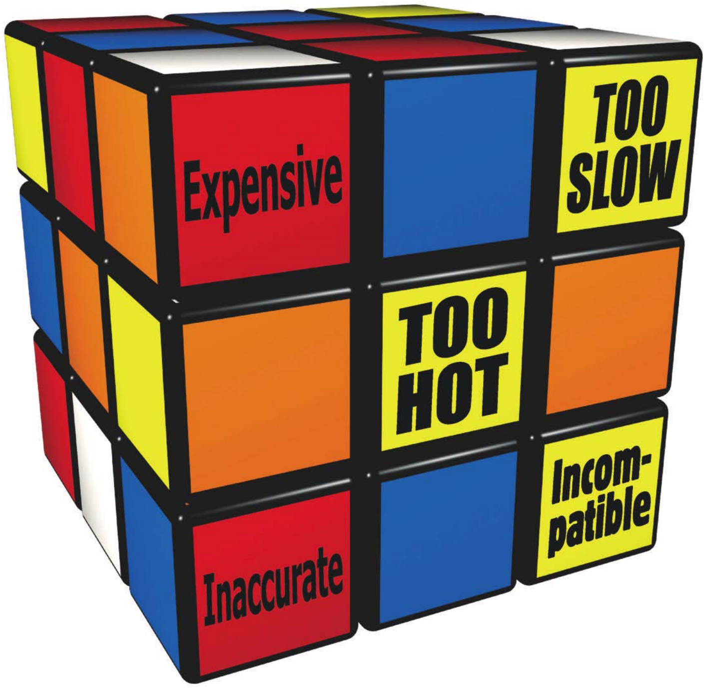

Expensive
TOO SLOW
TOO HOT
Incom-patible
Inaccurate


icemax
icechip
icepak
iceboard
icepro

The space-age material for the limited space age.

— or —

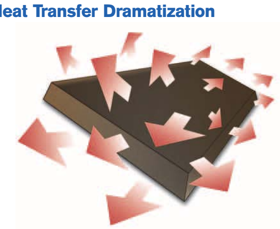
Why natural graphite is the best thermal solution for designing compact electronic devices.

As electronics get smaller and faster, design space becomes more critical. There simply is not room for traditional electronic cooling devices. Heat sinks, heat pipes and fans add weight, take up space, and are noisy. Traditional heat spreaders made of Cu and Al do not possess the properties for moving heat in a controlled, directional fashion that causes a shielding effect. And in compact devices you can not afford to have heat move from one source and adversely affect another. The solution? Expanded natural graphite – namely eGraf® SpreaderShield™ Heat Spreaders and eGraf® Fredda™ 3-Dimensional Heat Spreaders.

COOLER

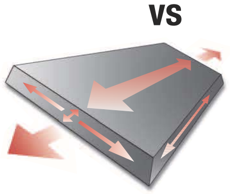
eGraf® materials are the latest technology available from GrafTech – global experts in expanded natural graphite thermal solutions. Expanded natural graphite solves problems associated with traditional heat management options. Compared to typical Al alloys, eGraf® components exhibit up to 200% higher thermal conductivity. The most dynamic characteristic of natural graphite is that it is anisotropic. Heat moves through it 2-dimensionally in an orderly fashion. The in-plane thermal conductivity is tailorable up

Heat Transfer Dramatization



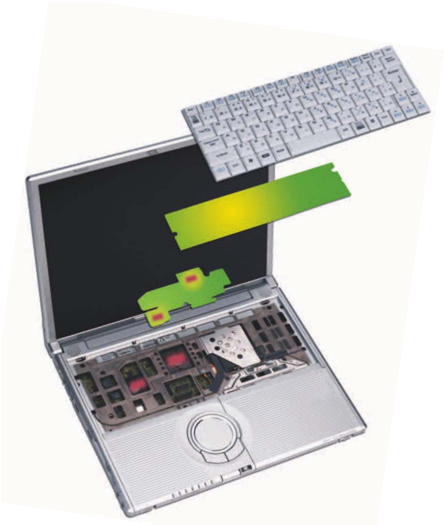
Isotropic Cu or Al has no thermal direction control or thermal shielding capability.

VS



Anisotropic eGraf® SpreaderShield™ material has full thermal direction control and thermal shielding capability.

LIGHTER



eGraf® materials eliminated the need for fan, heat pipes and heat sinks.

to 500 W/mK and the through-plane in the range of 5-10 W/mK. This allows engineers the ability to direct heat in the x-y plane. The result, our material spreads heat and also creates a thermal shielding barrier to keep heat from affecting other components. Some traditional Cu or Al spreaders cannot do this.

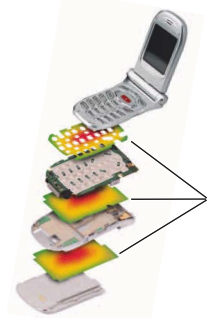
eGraf® offers an array of solutions for engineers faced with space, weight and thermal reliability issues. eGraf® SpreaderShield™ material is a thin sheet of flexible graphite that fits where traditional heat spreaders can not. It can be tailorable up to 500 W/mK and can be die-cut to fit applications of any size or shape. eGraf® expanded natural graphite's pliable qualities allow it to conform to any design. It is available in a variety of thicknesses and useable at temperatures up to 400°C and lower than -40°C.

For more complex 3-dimensional shapes, we laminate our eGraf® SpreaderShield™ material with a thin sheet of Al foil to hold form, creating eGraf® Fredda™, a 3-Dimensional Heat Spreader. eGraf® Fredda™ materials can conduct, spread and sink heat to the outer case of an electronic device for sealed environments. This can eliminate the need for heat pipes, heat sinks and fans in low and ultra low voltage applications, resulting in decreased assembly weight of those components up to 50%.

COST EFFECTIVE

Customized to fit your needs
200% better thermal performance than Al and 80% lighter than Cu

What are you designing? eGraf® SpreaderShield™ and eGraf® Fredda™ materials are already being used in ultra low/low voltage notebook computers, ruggedized computers, PDPs, LCDs, LEDs, audio amplifiers, avionics, consumer electronics, PDAs, smart cell phones, medical devices and much more.



eGraf® SpreaderShield™ material can be used in a variety of configurations for cell phones.

Challenge our thermal designers today to create thermal solutions on your next project. Just call, send us an email, or visit our website.

Phone: (800) 253-8003
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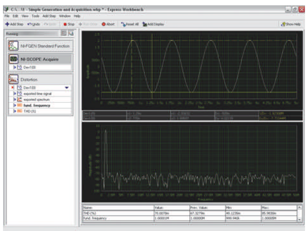
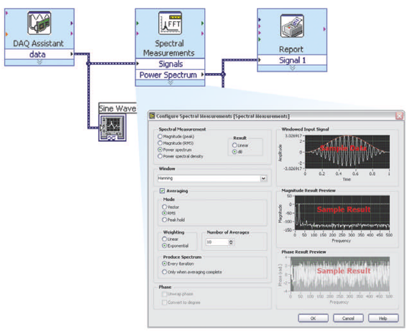
NI LabVIEW – From Interactive Measurements to Graphical System Design



Explore

Express technology in NI SignalExpress gives you an interactive, exploratory interface with:

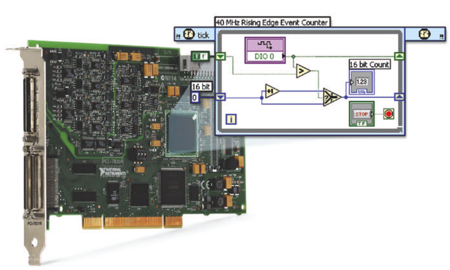
- Always-on, configuration-based development
- Tight integration of simulation and real-world I/O data
- Conversion to National Instruments LabVIEW projects



Configure

Point-and-click assistants in LabVIEW help you quickly automate common measurement and analysis tasks with:

- Modular data acquisition from DC to 2.7 GHz
- Plug-and-play drivers for more than 4,000 instruments
- Support for PXI, PCI, PCMCIA, USB, LAN, serial, GPIB, and CAN
- More than 450 signal processing and mathematics functions
- Drag-and-drop custom user interface (UI) design with built-in UI elements



Design

Revolutionary LabVIEW graphical programming helps you tackle the unique needs of your applications with:

- Compiled execution
- Intuitive dataflow development
- More than 500 included example programs, thousands more on the Web
- Advanced training classes and certification program
- Open connectivity with .NET, ActiveX, XML, TCP/IP, wireless, and more
- Integration with image acquisition and motion control devices
- Deployment to real-time, distributed, embedded, and handheld targets

Whether you are taking quick, interactive measurements on your desktop or designing sophisticated, high-throughput automated test systems, award-winning NI LabVIEW graphical software has the development tools you need. With more than 18 years of engineering innovation and thousands of users around the world, LabVIEW provides a scalable solution for your projects ranging from interactive design to custom application development.

To take the interactive LabVIEW Guided Tour, visit **ni.com/labview.**

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NATIONAL INSTRUMENTS™

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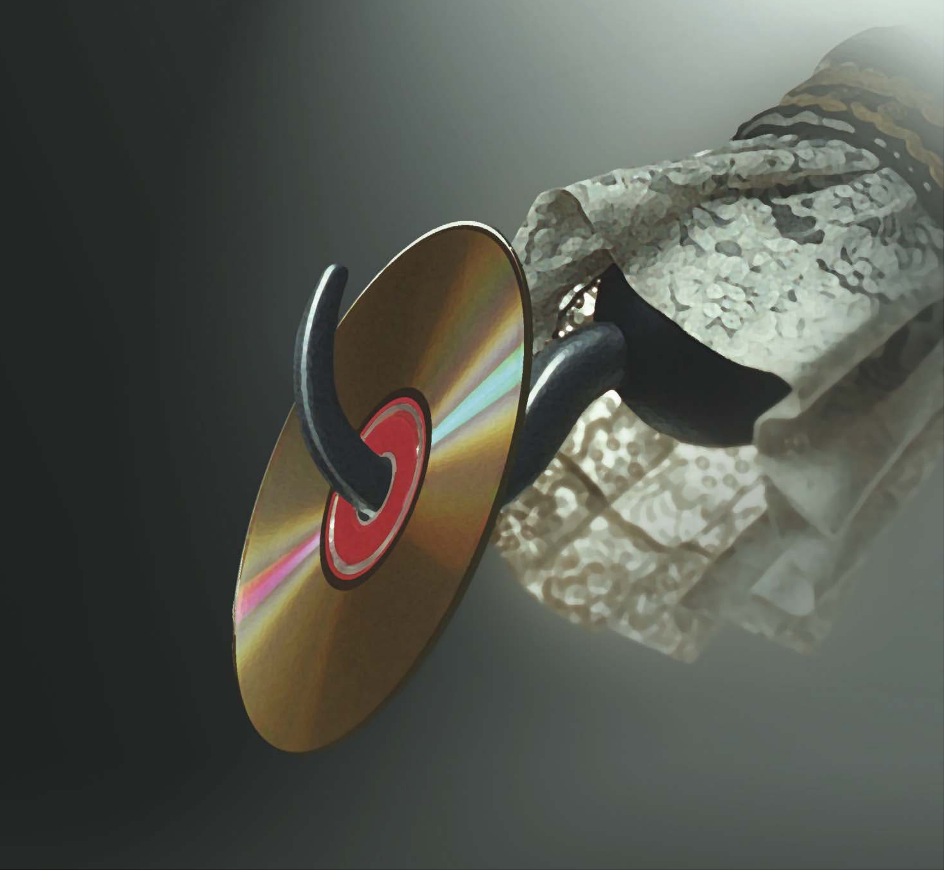
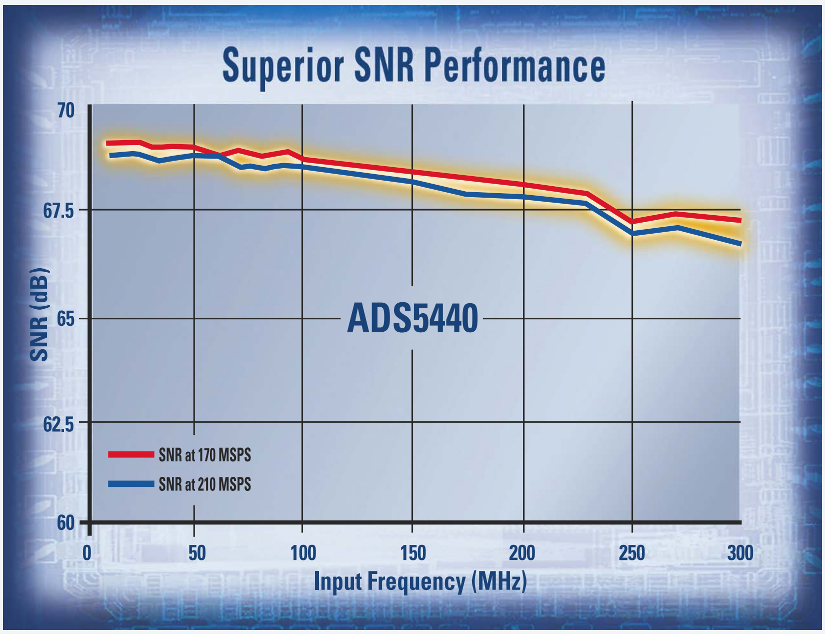


DATA CONVERTERS

13-Bit, 210 MSPS ADC

Superior SNR Performance. Now!



The **ADS5440** high-speed analog-to-digital converter from Texas Instruments features superior dynamic performance at high input frequencies. Providing break-through SNR performance, the ADS5440 enables improved receiver performance in multi-channel base stations and software defined radio (SDR) applications, and improved sensitivity for test and measurement equipment.

Device	Resolution (Bits)	Speed (MSPS)	SNR (dBc)	SFDR (dBc)
ADS5440	13	210	68 at 170 MHz IF	77 at 170 MHz IF
ADS5500	14	125	69.5 at 100 MHz IF	82 at 100 MHz IF
ADS5424	14	105	74 at 50 MHz IF	93 at 50 MHz IF
ADS5541	14	105	71 at 100 MHz IF	86 at 100 MHz IF
ADS5423	14	80	74 at 50 MHz IF	94 at 50 MHz IF
ADS5520	12	125	68.7 at 100 MHz IF	82 at 100 MHz IF
ADS5521	12	105	69 at 100 MHz IF	86 at 100 MHz IF

▶ Applications

- Software defined radio
- Test and measurement/ instrumentation
- Base stations:
  - Multi-channel receivers
  - Transmit digital pre-distortion (DPD)
- Communication Instrumentation

▶ Features

- SNR = 68 dBc at 170 MHz F_{IN} and 210 MSPS
- SFDR = 77 dBc at 170 MHz F_{IN} and 210 MSPS
- SNR = 68 dBc at 230 MHz F_{IN} and 170 MSPS F_S
- SFDR = 80 dBc at 230 MHz F_{IN} and 170 MSPS F_S
- Supports the industrial temperature range of –40° C to +85° C
- 80-pin TQFP PowerPAD™ package
- Fully buffered input simplifies input circuit design
- Lead (Pb)-free/green
- $65.00/1K price

Evaluation Modules, Datasheets and Samples

www.ti.com/ads5440 ◦ 800.477.8924, ext. 12495

Technology for Innovators™ TEXAS INSTRUMENTS

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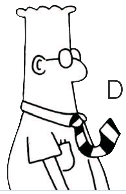
pulse



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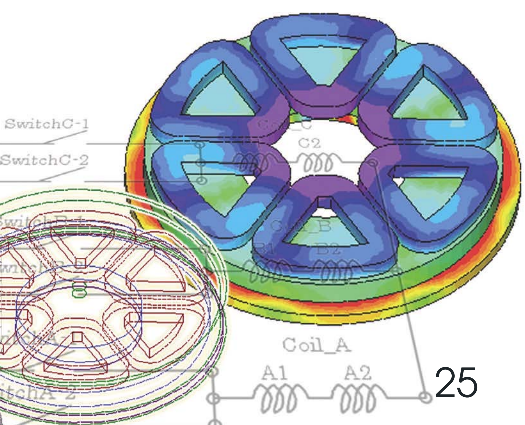

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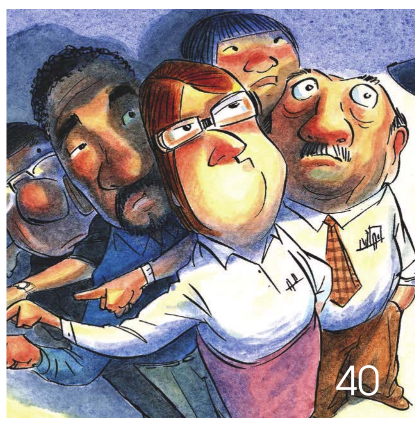

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DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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EDN online contents

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ONLINE ONLY

Check out these online-exclusive articles:

Bluetooth-stereo-headphone design cuts cord, power

Cambridge Silicon Radio (CSR) has released a reference design for Bluetooth stereo headphones, which is based on the company's BlueCore3-Multimedia chip (BC3-MM).
→www.edn.com/article/CA629473

No SOC is an island

Designers must look beyond the confines of the SOC and pay attention to integration with external chips and systems.
→www.edn.com/article/CA628274

Connector system skimps on board space

AVX has rolled out an I/O connector system designed for space-constrained applications including consumer electronics and medical equipment.
→www.edn.com/article/CA629491

Computer-on-module spec promises embedded flexibility

The PICMG has rolled out the COM (computer-on-module) Express Specification, known as COM.0, an open standard for small-form-factor add-on modules in embedded applications.
→www.edn.com/article/CA629490

Gear: Postcards from the edge of product evolution

Our regular peek at notable new digital-consumer products: pocket-sized wireless routers, tricked-out video decks, a 30-Gbyte camcorder, and more.
→www.edn.com/article/CA632101

Highly charged discussion

When Editor at Large Maury Wright recently used his blog to post some comments about the delivery of broadband by means of power lines (so-called BPL technology), he touched a live wire. Reader responses ran the gamut from "Access BPL will change the third world" to "Power lines were never designed for and cannot be made to carry broadband signals without creating massive interference to radio communications."

What do you think?
→www.edn.com/ontheverge

Tell your *Tale*, earn a $200 American Express gift check

Submit your own **Tale from the Cube**, and, if we accept it for publication, you'll receive a $200 American Express gift check. Check out this issue's installment (pg 40) and the examples below, then contact Editor at Large Maury Wright (mgwright@edn.com) with your Tale.

Watching the currents flow
→www.edn.com/article/CA624946

Baby steps stop the crying
→www.edn.com/article/CA608177

FROM THE VAULT

Articles and extras from the EDN archives that relate to this issue's contents.

"Compare Spice-model performance" (pg 38): This column by Ron Mancini is just the latest in an informative (and, judging by Web traffic, popular) series on the topic:

Validate Spice models before use
→www.edn.com/article/CA512147

Understanding Spice models
→www.edn.com/article/CA514958

Verify your ac Spice model
→www.edn.com/article/CA601850

Beyond the Spice model's dc and ac performance
→www.edn.com/article/CA608176

"VNAs and TDRs: taking the measure of the new millennium" (pg 61): This article touches on Smith charts, which Executive Editor Bill Schweber covered in detail in 1999:

The Smith chart: More vital after all these years

The original Smith chart—60 years after its development—is an increasingly important tool for the RF aspects of any design.
→www.edn.com/article/CA56700

"Power goes digital" (pg 75): Joshua Israelsohn took an in-depth look at digital power control in the July 21 issue:

A bit-o'-power: digitally controlled power conversion

Digital power control may bring performance benefits to some applications, but until you become familiar with the inner machinations, their sophistication will exact a price in application-development time.
→www.edn.com/article/CA6249510


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BY JOHN DODGE, EDITOR IN CHIEF

Where land does not meet the sea

Who pays for the software piracy that Senior Editor Mike Santarini's cover story so ably analyzes? You and I. We are constantly subjected to frustrating protection schemes that cost time and money. Perhaps that's a small price to pay given the magnitude and seriousness of the piracy problem, but I couldn't help recall a stressful experience installing marine navigational maps on a Magellan Meridian handheld GPS device.

To "unlock" a specific marine chart from a CD, I had to perform a series of time-consuming and obnoxious steps triggered by denial of access to the software I had just paid for. First, I had to open a useless Web account with the supplier that required answers to marketing questions. It wasn't just annoying; it made me feel like a criminal.

Next, I had to enter a 20-digit serial number from the software to gain access to an equally unfathomable string of numbers called an unlock code (**Link 1**). It gets worse.

That code, as it turned out, did its unlocking thing only when matched up with two more specific serial numbers—the one on the SD memory chip in the handheld and the handheld's own serial number. The goal of this system is to prevent charts from being downloaded into all but the one assigned GPS handheld device containing the one assigned SD memory card inside the unit.

During this grinding process, entering an incorrect digit was almost guaranteed, so when I stumbled, I was forced to call (Magellan parent company) Thales Navigations' customer-support line for help. To its credit, a tech called back right away, but if you hang on the line for one, wait times are 90 minutes or more.

I had to erase one chart if I wanted to download another.

The tech had more bad news. I could not install any of the 20 marine charts from the BlueNav CD I bought for $130 on the same SD memory chip that held my detailed street data from the MapSend CD for which I had doled out an equal sum. Land and sea had to be on separate SD chips lest marine files swamp (err, corrupt) the street files, I was told. What nonsense! Moreover, I could not download more than one chart at a time onto the assigned marine SD chip. In others words, I had to erase one chart if I wanted to download another, even though the chip's capacity was enough to hold a half-dozen charts or more.

The scheme is hopelessly restrictive and dysfunctional. If you're confused, you fully understand what I was up against.

Granted, detailed digital maps are prime targets for pirating, but they have always been overpriced—although now, the consumer gets more for the money. The manufacturer's suggested retail price for a Magellan chip with a bit more than the entire Maine coast is $200. A few years ago, $200 bought you maybe 30 to 40 miles of coastline. Customers have the option of buying chips with charts already on them or a CD with all the charts and downloading them individually onto a blank chip.

The charts are still pricey, but they can save your life, and the Magellan Meridian Platinum handheld is a dynamite product, consistently prevailing over rivals in Amazon's all-important customer reviews.

Clearly, software vendors feel desperate enough to go to such lengths to protect their assets. When it comes to business software or EDA tools, the cost of doing business includes using encryption schemes and keys that protect against unauthorized use and reproduction to the extent possible. And, given that an estimated 90% of all software in China is stolen, the logical me understands why Thales went to such extremes. However, the customer me filled with scorn at mere mention of the company's name.

The best of the worst piracy schemes I recall was the proposed Ashton-Tate worm that destroyed hard drives if it detected a pirated version of the company's dBase database software (**Link 2**). Someone in the 1980s floated but never launched this bad if not illegal idea. Even so, the chief executive officer at the time received ridicule and harsh criticism for even considering it.

Yes, software piracy is bad and must be stopped. But in the process of protecting resources, vendors must be as cognizant of their customers as they are of the pirates. EDN

WEB LINKS

1 www.magellangps.com/en/products/keys.asp.

2 www.hodgy.net/computer_history/page_2/page_2.htm.

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Vol. III, Issue 8

ANALOG | edge℠

DESIGN | *idea:* Serial LVDS Improves Routing ▶▶

Featured Products

Differential, High-Speed Op Amps

The LMH6550 and LMH6551 are high-performance voltage feedback differential amplifiers. The fully differential topology allows balanced inputs to the ADCs and can be used as single-ended-to-differential or used as differential-to-differential. These amplifiers also have the high speed and low distortion necessary for driving high-performance ADCs, as well as the current-handling capability to drive signals over balanced transmission lines like CAT-5 data cables. The LMH6550/51 can handle a wide range of video and data formats.

With external gain set resistors, the LMH6550/51 can be used at any desired gain. Gain flexibility coupled with high speed makes these amplifiers suitable for use as IF amplifiers in high-performance communications equipment.

LMH6550 Features

- 400 MHz, -3 dB bandwidth (V_{OUT} = 0.5 V_{PP})
- 90 MHz, 0.1 dB bandwidth
- -92/-103 dB HD2/HD3 at 5 MHz (changed order)
- 3000 V/µs slew rate
- -68 dB balance error (V_{OUT} = 1.0 V_{PP}, 10 MHz)
- 10 ns shutdown/enable

LMH6551 Features

- 370 MHz, -3 dB bandwidth (V_{OUT} = 0.5 V_{PP})
- 50 MHz, 0.1 dB bandwidth
- -94/-96 dB HD2/HD3 at 5 MHz (changed order)
- 2400 V/µs slew rate
- -70 dB balance error (V_{OUT} = 0.5 V_{PP}, 10 MHz)
- Single +3.3V, +5V, or ±5V supply voltages

The LMH6550/51 is ideal for use in applications requiring a differential A/D driver, video twisted pair, differential line driver, single end-to-differential converter, high-speed differential signaling, IF/RF amplifier, or SAW filter buffer/driver.

The LMH6550/51 are available in the space-saving SOIC-8 and MSOP-8 packaging.

www.national.com/pf/LM/LMH6550.html
www.national.com/pf/LM/LMH6551.html

Low-Power, High-Performance Quad 12-Bit A/D Converter with Serialized LVDS Outputs

The ADC12QS065 is a low-power, high-performance, 4-channel analog-to-digital converter with serialized LVDS outputs. This A/D converter digitizes signals to 12-bit resolution at sampling rates up to 65 MSPS while consuming a typical 187.5 mW per ADC from a single 3.0V supply. Sampled data is transformed into high-speed serial LVDS output data streams. Clock and frame LVDS pairs aid in data capture. The six differential pairs of the ADC12QS065 transmit data over backplanes or cable and simplify PCB design. In addition, the reduced cabling, PCB trace count, and connector size greatly reduce system cost.

Features

- Serialized LVDS outputs allow for lower pin count packages
- Saves space for number of channels
- Pin assignment optimized for board layout
- Low power consumption
- Excellent signal-to-noise ratio, THD, and crosstalk
- Samples signals as fast as 65 MSPS

The speed, resolution, and single-supply operation of the ADC12QS065 make it well suited for a wide variety of applications in ultrasound, medical imaging, communications, portable instrumentation, and digital video.

Operating over the industrial (-40°C to +85°C) temperature range, the ADC12QS065 is available in a TQFP-64 package.

www.national.com/pf/DC/ADC12QS065.html

National Semiconductor
The Sight & Sound of Information

DESIGN | *idea*

Robert LeBoeuf
Senior IC Design Engineer
National Semiconductor

Data Converter Serial LVDS Interface Improves Board Routing

Systems often require signaling where common-mode signals are not welcome or difficult to handle. Some designs turn single-ended signals from the output of transducers to fully differential signals, then send this signal to a differential-input ADC downstream. The advantage of this is that most noise that gets introduced on this differential line is common to both lines. (This is assuming that the differential lines are laid out symmetrically.)

After the input signals are converted to digital data, they must be transmitted to a DSP or an ASIC/FPGA for processing. This is where fully-differential output signaling can come in handy. Output signals that are fully differential source and sink a current through two symmetric lines. An example of such signaling is the LVDS (Low Voltage Differential Signal) format. The ADC12QS065 uses LVDS to solve all of these system issues (***Figure 1***).

The ADC12QS065 contains four 12-bit ADCs in one chip. Each of its inputs accepts fully-differential signals. The input common-mode voltage may be derived from the common-mode output reference voltages VCOM12 and VCOM34 that are supplied by the ADC12QS065. The ADC12QS065 also has the option of using a fully-differential, or single-ended clock source. To utilize the LVDS clock simply provide LVDS signals to the CLK and CLKB, terminating close to the input

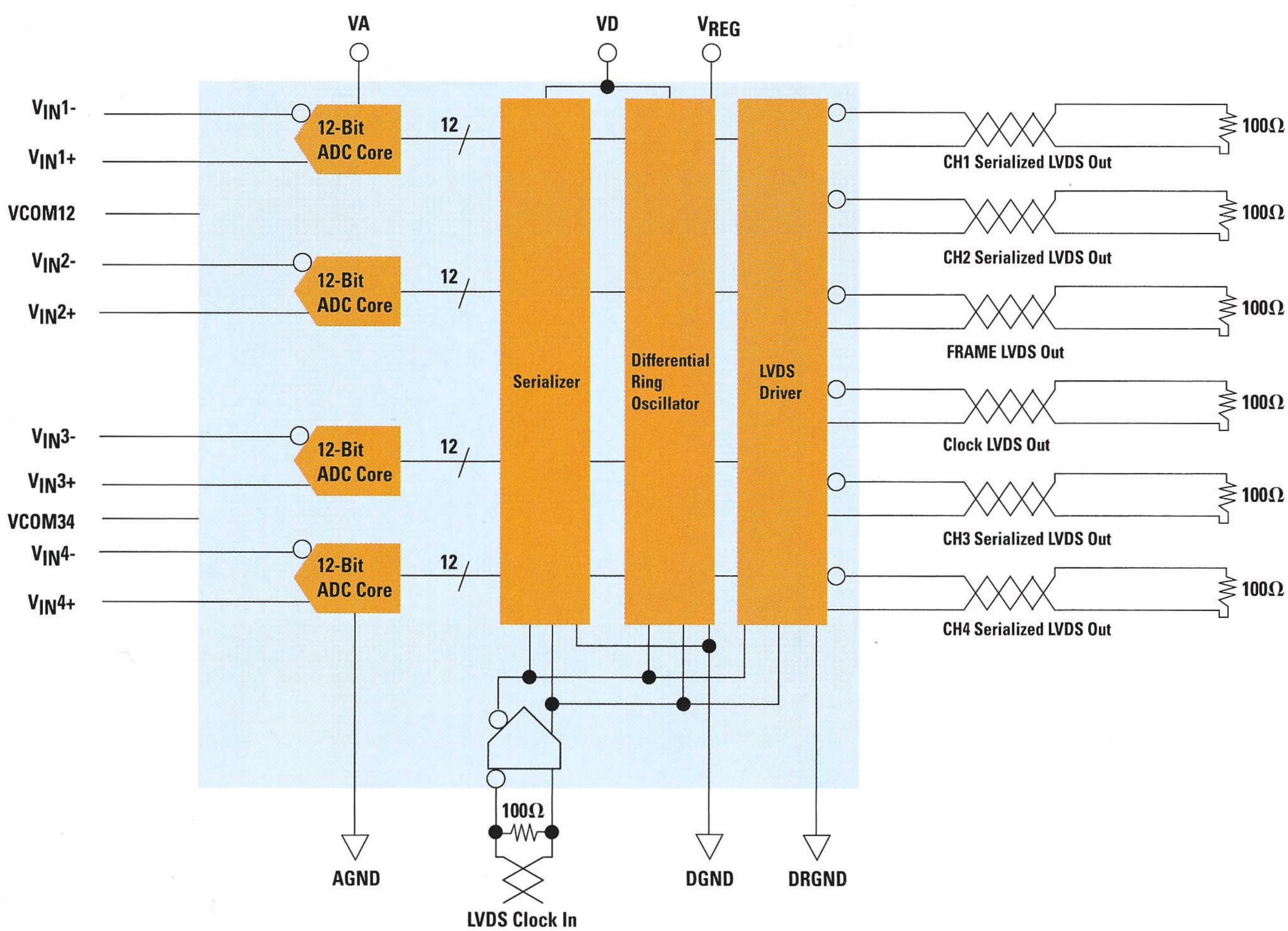


Figure 1. ADC12QS065 Simplified Block Diagram

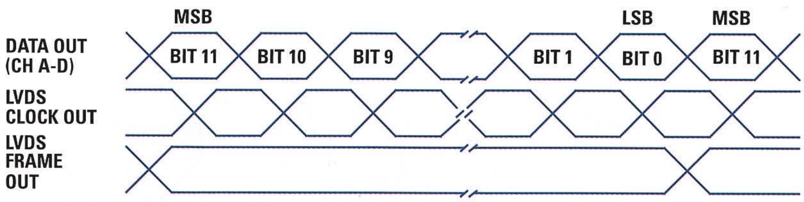


Figure 2. Output Timing Diagram

pins. If a single-ended CMOS clock is desired, then CLKB is tied low, and no termination resistor is required.

The output of each ADC gets serialized using a differential ring oscillator. The input clock input is multiplied by 12, and converted to an LVDS clock output for data capture. An LVDS FRAME signal, at the input clock rate, is also generated at the output to identify the sample number (***Figure 2***).

The output timing offers easy data capture for an FPGA. The output FRAME signals when sampled data is ready to be sent. The MSB of each of the 4 output channels is present, followed by an LVDS CLOCK OUT transition. The LVDS CLOCK OUT signal is offset from the DATA OUT by a quarter cycle to ease clock management. Each data bit is captured on a CLOCK OUT transition. Another advantage of using LVDS is that these signals may be sent down a twisted pair that uses the EIA/TIA 568 standard. Twisted pairs that meet this standard have a characteristic impedance of 100Ω. Conductors that are close together and carry opposite currents produce very low radiation. This is welcome in areas where high SNR requirements are present.

To further illustrate this point, ***Figure 3*** shows two 4-channel, 12-bit ADCs. The ADC on the left has the traditional single-ended parallel CMOS output. 49 traces are required (4x12+1) to send the converter output to the digital processor. If the output bits are serialized, each channel would have a single pair of differential lines. An output clock and frame signal wires are also illustrated.

Because LVDS uses current from the supply by 'steering' current from one LVDS terminal or the other, current is constantly being drawn from the supply. This reduces the switching load that would otherwise be present on the supply lines. The advantage to this is that lower supply noise is induced on the supply line, reducing the decoupling capacitor size, and relaxing layout requirements.

Serial LVDS allows for an even smaller package and is very effective in signal transmission. In many applications, however, low power consumption is very important. Every milliwatt of power saved per channel makes a significant difference in systems requiring several channels of data. Therefore, in addition to quiet drivers, the ADC12QS065 has three separate power supplies. Each supply can be connected making it a single-supply ADC, or kept separate. Separate supplies further isolate each part of the internal circuitry of the ADC. This may be achieved with one supply and passive filters employed at each power supply input, or separate supplies altogether. Another advantage separate supplies is the output driver voltage may be reduced as low as 2.5V, to save on power consumption.

The ADC12QS065 also has the ability to have its internal references powered down to allow the reference to be driven externally. This allows multiple ADCs to be 'ganged' together, by connecting all the V_{REF}Ps and V_{REF}Ns together, respectively. This eases system calibration requirements by helping to insure that the gain and offset of each chip match.

It's clear that if systems allow for differential signaling, it is advantageous in terms of low common-mode noise induction, reduced power supply transients, and low digital radiation on the output lines. The ADC12QS065 offers a fully-differential conversion, from the analog input, clock input, to the serialized LVDS outputs. This ability to separate the power supplies allows for further analog-digital domain separation, and offers lower power consumption. ■

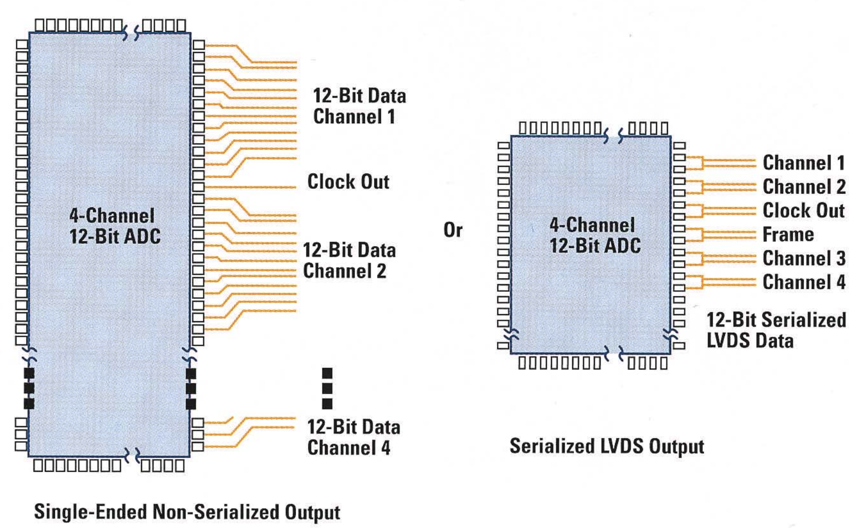


Figure 3. CMOS vs LVDS Board Layout Comparison

Featured Products

High-Performance, Low-Power, Dual 8-Bit, 500 MSPS A/D Converter

The ADC08D500 is the industry's lowest power dual 8-bit 500 MSPS analog-to-digital converter. It digitizes two signals to 8-bit resolution at sampling rates up to 800 MSPS or one signal at sampling rates up to 1.6 GSPS. Consuming a typical 1.4 W at 500 MSPS from a single 1.9V supply, this device is guaranteed to have no missing codes over the full operating temperature range. The unique folding and interpolating architecture, the fully differential comparator design, the innovative design of the internal sample-and-hold amplifier, and the self-calibration scheme enable a very flat response of all dynamic parameters beyond Nyquist.

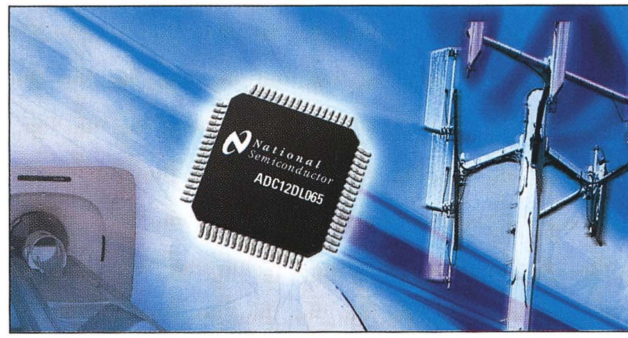
Features

- 7.5 Effective Number of Bits (ENOB) at Nyquist (typ)
- Bit error rate 10^{-18} (typ)
- Single +1.9V (±0.1V) operation
- Interleave mode for 2x sampling rate
- Choice of SDR or DDR output clocking
- Multiple ADC synchronization capability
- Serial interface for extended control
- Fine adjustment of input full-scale range and offset

The ADC08D500 is ideal for use in direct RF down conversion, digital oscilloscopes, satellite set-top boxes, communications systems, and test instrumentation.

This A/D converter is available in a thermally-enhanced exposed pad LQFP-128 and operates over the industrial (-40°C to +85°C) temperature range.

www.national.com/pf/DC/ADC08D500.html



Dual 12-Bit, 65 MSPS, 3.3V, 360 mW A/D Converter

The ADC12DL065 is a dual, low-power CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 65 MSPS. This converter uses a differential, pipeline architecture with digital error correction and an on-chip sample-and-hold circuit to minimize power consumption while providing excellent dynamic performance and a 250 MHz full power bandwidth. Operating on a single +3.3V power supply, the ADC12DL065 achieves 11.0 effective bits at Nyquist and consumes just 360 mW at 65 MSPS, including the reference current. The power down feature reduces power consumption to 36 mW.

Features

- 11.0 ENOB at Nyquist (typ)
- SNR = 68.5 dBc with f_{IN} = 10 MHz (typ)
- SFDR = 85 dBc with f_{IN} = 10 MHz (typ)
- Consumes only 360 mW at 65 MSPS
- Outputs 2.4V to 3.6V compatible
- Power down mode
- Duty cycle stabilizer
- Multiplexed output mode simplifies board routing

The ADC12DL065 is ideal for use in ultrasound and imaging, instrumentation, communications receivers, sonar/radar, xDSL, cable modems, and DSP front ends.

This device is available in a TQFP-64 package and will operate over the industrial temperature range of -40°C to +85°C.

www.national.com/pf/DC/ADC12DL065.html

Intersil Interface Products

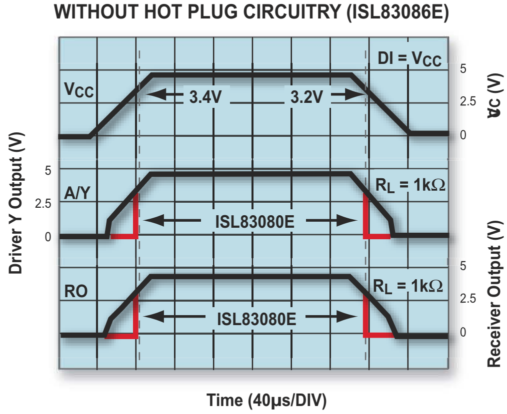
Intersil High Performance Analog

Want a More Dependable Bus?

Try a better Transceiver. Intersil's new ISL8308XE 5V Fractional (1/8) Unit Load, RS-485/RS-422 Transceivers incorporate "Hot Plug" functionality to keep your bus from crashing during power-up and power-down.

That's not all. These devices feature 15kV ESD Protection; "Full Fail-Safe" design to ensure a high Rx output if Rx inputs are floating, shorted, or terminated but undriven; and low bus currents to allow up to 256 transceivers on the network without violating the RS-485 network specification's 32 unit load maximum without using repeaters.

HOT PLUG PERFORMANCE (ISL83080E) vs DEVICE WITHOUT HOT PLUG CIRCUITRY (ISL83086E)



Key Features:

- True 1/8 Unit Load allows up to 256 devices on the bus
- Hot Plug circuitry to maintain three-state Tx and Rx outputs during power-up and power-down
- Full Fail-Safe (open, short, terminated and floating) receivers
- ±15kV HBM ESD Protection on RS-485 I/O pins and Class 3 ESD Protection on all pins
- Available in Pb-Free and small MSOP packages

Datasheet and more info available at **www.intersil.com/edn**

5V, High ESD, Fractional (1/8) Unit Load RS-485/RS-422 Key Specifications

Device	# of Tx/ # of Rx	Devices Allowed on Bus	Half/ Full Duplex	High ESD?	Hot Plug?	Data Rate (Mbps)	Slew Rate Limited?	Tx/Rx Enable?	ICC EN / DIS (µA)	SHDN ICC (µA)	VCC Range (+V)	Pkg.
ISL83080E	1 / 1	256	Full	Yes	Yes	0.115	Yes	Yes	530 / 530	0.07	4.5 to 5.5	14 Ld SOIC
ISL83082E	1 / 1	256	Half	Yes	Yes	0.115	Yes	Yes	560 / 530	0.07	4.5 to 5.5	8 Ld MSOP 8 Ld SOIC
ISL83083E	1 / 1	256	Full	Yes	Yes	0.5	Yes	Yes	530 / 530	0.07	4.5 to 5.5	14 Ld SOIC
ISL83085E	1 / 1	256	Half	Yes	Yes	0.5	Yes	Yes	560 / 530	0.07	4.5 to 5.5	8 Ld MSOP 8 Ld SOIC
ISL83086E	1 / 1	256	Full	Yes	No	10	No	Yes	530 / 530	0.07	4.5 to 5.5	14 Ld SOIC
ISL83088E	1 / 1	256	Half	Yes	No	10	No	Yes	560 / 530	0.07	4.5 to 5.5	8 Ld MSOP 8 Ld SOIC

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EDITED BY FRAN GRANVILLE

pulse

INNOVATIONS & INNOVATORS

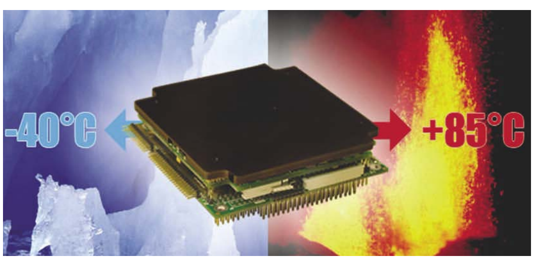
Fanless CPUs tackle extremes

Parvus recently introduced three ruggedized, 800-MHz Pentium-based embedded-processor boards for demanding mobile, high-vibration, and extreme-temperature computing applications. The PC/104-Plus-form-factor CPU cards each incorporate an Intel ULV (ultralow-voltage) Tualatin Pentium III processor, an Intel 815E chip set, and select peripherals. The devices include the SpacePC CPU-1460, which includes standard embedded-PC-peripheral devices; the SpacePC CPU-1461, which supports as many as eight USB devices, six of which comply with high-speed USB 2.0; and the SpacePC CPU-1463, which features dual network controllers, including a Gigabit Ethernet interface and a 10/100-MHz Ethernet controller.

Each module employs a flat, aluminum heat-spreader plate on top of the processor boards so that sealed embedded systems can reliably operate at −40 to +85°C without a fan. The modules are also hardware-compatible with most popular real-time operating systems, including Windows CE, Windows XP Embedded, Linux, QNX Neutrino, and VxWorks. The CPU-146X models are available now for $1023 to $1253 (100).

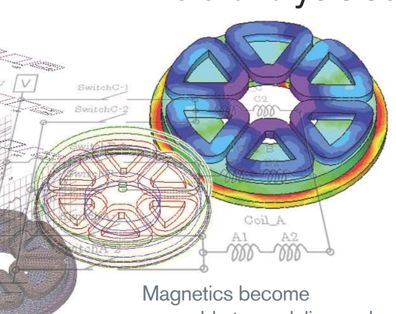
—by Warren Webb

▷**Parvus Corp**, www.parvus.com.



Three new ruggedized PC/104-Plus CPU boards from Parvus integrate the low-power Intel Pentium III processor with multiple peripheral options.

Field-analysis software is the EDA of magnetic designs



Magnetics become amenable to modeling and simulation with the JMAG-Studio tool from Japan Radio, available in the United States from Motorsoft.

Software-design tools are not just for IC and pc boards; designers of motors, inductors, generators, and solenoids also benefit from the assistance of the advanced modeling, design, and simulation tools. JMAG-Studio from the Japan Radio Institute (www.njr.co.jp) is now available in the United States through the Motorsoft Division of Fisher Electric Technology. It provides magnetic-field analysis for 2- and 3-D, static and transient problems. The program's models yield magnetic flux, flux density, EM force, torque, stored energy, current density, loss, impedance, inductance, voltage, and other parameters.

Designers can use the well-known Solidworks (www.solidworks.com) CAD package as the source of the input data for the 3-D analysis. The automatic mesh function provides the optimal mesh for the magnetic analysis. The 2- and 3-D standard packages sell for $16,000 and $18,400, respectively.**—by Bill Schweber**

▷**Motorsoft/Fisher Electric Technology**, www.motorsoft.com.

MAGNETIC ENCODER OFFERS EXTREME NONCONTACT RESOLUTION

Using a technology similar to a magnetic tape or disk platter, the Siko Products MSK5000 linear/rotary encoder is a 5-mm-wide band with programmable resolution to 1 micron (0.001 mm). In contrast to optical systems, this approach resists dirt and contamination, accepts larger misalignment tolerances, and has a wider temperature range. The flexible, adhesive-backed band is straightforward to install, and the integrated translation-unit read head includes status LEDs and setup indicators. Read distance, or ride-height run-out, can be as much as 2 mm. The price for a linear or a radial encoder tape and read head starts at approximately $200.

—by Bill Schweber

▷**Siko Products Inc**, www.sikoproducts.com.

For precise linear and rotary sensing, the magnetic-based MSK5000 offers resolution to 0.001 mm and a read distance as long as 2 mm. It remains unaffected by dirt, which can impede optical-sensing approaches.

ICs enable analog video to give and receive

Despite the digital nature of many video signals, they often need to live in the analog RGB/YPbPr world, alongside the line drivers and receivers that make that world possible. The ISL59830 IC from Intersil facilitates this collaboration. The single-supply, triple-video driver internally generates its requisite negative supply, thus eliminating the need for a negative-supply rail and dc-blocking capacitors.

Pay attention, you digital-system designers: In the arcane world of video architectures, circuits use either ac or dc interstage coupling. The ac approach needs relatively large external capacitors but no negative supply; the dc approach requires a bipolar supply but no capacitors. According to Sameer Vuyyuru, director for high-speed analog at the company, "The video driver is often the only product in a design that still requires a negative-supply rail where dc accuracy is required."

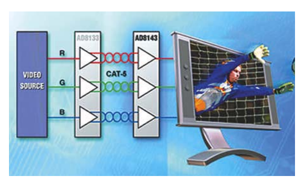
The 3.3V IC has built-in fixed-gain-of-two (6-dB) buffers and three-state outputs, designed to drive 75Ω, double-terminated lines. Bandwidth is 50 MHz at 0.1-dB flatness and 300 MHz at 3 dB for the 16-lead devices, which are available for $1.88 each (1000).

Line driving alone is only part of the video-signal chain. Analog Devices' AD8143 triple differential receiver lets designers use Category 5 unshielded twisted-pair cable rather than more expensive coaxial cabling for RGB signals with resolution as high as 1600×1200 pixels. Designers can also use the IC for general differential-analog or high-speed data signals. The IC converts differential signals to single-ended signals with a common-mode range of ±10V to maintain signal integrity despite large ground-potential difference. CMRR (common-mode-rejection ratio) is 70 dB at 10 MHz.

In addition to the line receivers, the device contains two comparators, which can sense digital signals from the unused fourth pair in the cable. A typical use would be to handle keyboard and mouse signals in KVM (keyboard/video/mouse) applications. The AD-8143, a 5×5-mm, 32-lead device, sells for $2.55 (1000) and is the complement to the AD8133 triple-differential line driver.—**by Bill Schweber**

▷**Intersil Corp**, www.intersil.com.

▷**Analog Devices Inc**, www.analog.com.



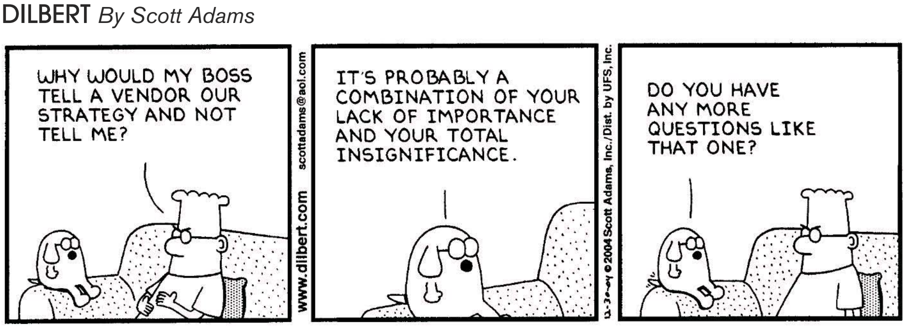
The latest ICs ease the task of analog-video-line driving and receiving: The Intersil ISL59830 triple driver requires no negative supply or blocking capacitors (left), and the Analog Devices AD8143 triple receiver lets systems operate with Category 5 twisted-pair cabling rather than more expensive cables (right).

FEEDBACK LOOP

"I do feel badly for the brighter high school students to whom electrical engineering might have offered a solid technical future."

Rudy Dankwort, in *EDN*'s Feedback Loop on www.edn.com/article/CA526328. Add your comments.

DILBERT *By Scott Adams*



08.18.05

$30 module embeds speech recognition

Sensory recently unveiled the VR Stamp module, which provides easy integration of voice recognition into consumer, industrial, automotive, and medical electronics. Sensory based the module on the company's RSC-4128 mixed-signal processor, which includes an 8-bit microcontroller, an ADC, a DAC, digital filtering, RAM, ROM, and output amplification. The device also packs flash memory, serial EEPROM, clock crystals, and noise-management components into its standard, 40-pin DIP footprint.

Sensory's FluentChip software provides speech recognition, speaker verification, speech compression and output, music synthesis, and diagnostic and utility programs. Bill Teasley, Sensory's vice president of engineering, says, "The VR Stamp makes it practical for developers to incorporate voice recognition and speech synthesis as the human interface to any product. Imagination is the only limitation." The VR Stamp modules sell for less than $30 (high volumes). Sensory also offers a $495 VR Stamp tool kit and programming board to simplify the development of speech command sets, speech-synthesis prompts, and end-product circuit design.—by Warren Webb

▶**Sensory Inc, www.sensoryinc.com.**

Embedded computer packs extra I/O

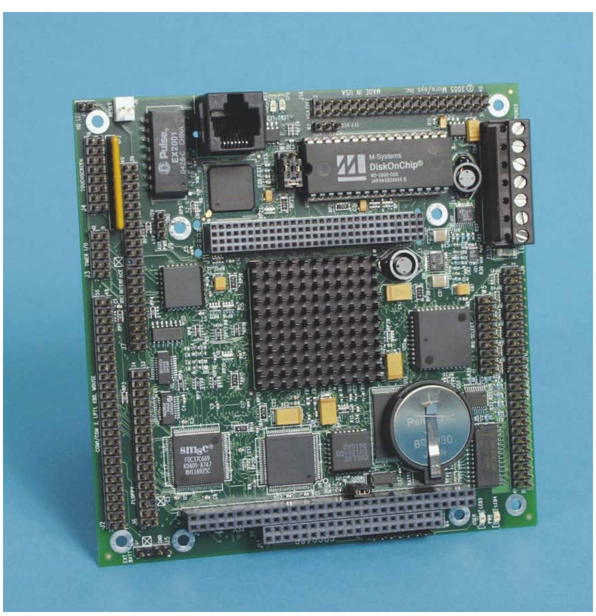
Micro/sys based its new SBC0489 single-board computer on the STPC Atlas PC-compatible processor. The device delivers an I/O-rich single-board computer in a 5×5-in. footprint. Along with expected PC features, such as SVGA and disk controllers, the board also includes digital I/O, ADCs, DACs, and Ethernet support. With 64 Mbytes of RAM and as much as 128 Mbytes of flash, SBC0489-based systems can run applications requiring headless and diskless configurations as well as full disk-based GUI systems.

The SBC0489 includes COM1, COM2, LPT1, keyboard, mouse, floppy, IDE, and 8×8-key matrix touchscreen or keypad interfaces. A Super-VGA interface drives CRT monitors and active-matrix flat-panel displays with resolutions as high as 1024×1024 pixels. Application I/O includes 10/100-MHz Ethernet; 24 CMOS I/O lines from an 82C55; an eight-channel, 12-bit ADC; a four-channel, 12-bit DAC; and three 16-bit timers from an 82C54. Designers can add I/O expansion if necessary to the SBC0489 through both PC/104 and PC/104-Plus cards.

The SBC0489 can boot DOS, Linux, Windows CE, and other PC-compatible operating systems. The company ships a free development kit, which includes cables, sample software, and full documentation, with the board. Prices for the basic SBC0489 start at $595 (one).

—by Warren Webb

▷**Micro/sys Inc**, www.embeddedsys.com.



The SBC0489 single-board computer mates a PC-compatible processor with analog I/O, digital I/O, and 10/100-MHz Ethernet interfaces.

MOTOR CONTROLLERS EASE DO-IT-YOURSELF CHALLENGE

08.18.05

Having a good motor is one thing; controlling the motor properly is another. The $850 Silverdust IGB from Quicksilver Controls provides servo control for NEMA 17 and 23 frame-sized microstep motors with encoders. Using this controller, you can achieve the performance of a four-quadrant servomotor but with a lower cost, two-phase motor. In addition, you can program the unit for advanced profiles, PID and velocity servo modes, and other motion-specific operations. It includes connections for power and communications, plus 16 isolated, 5 to 24V-dc, bidirectional I/O lines and four analog inputs.

For network-based, multiaxis motion supervision, the Maestro servoamplifier from Elmo Motion Control provides synchronized control, interpolated 2- and 3-D control, sequencing, and event handling, all as a CANopen Master. It operates as an Ethernet-to-CAN (controller-area-network) gateway with connectivity to a host PC or machine-control programmable-logic controller, with monitoring through a Web browser. Available software tools, which come with the unit, support application development and network installation. The basic unit sells for $1400.—by Bill Schweber

▶**Quicksilver Controls Inc, www.quicksilvercontrols.com.**

▶**Elmo Motion Control Inc, www.elmomc.com.**

It's all about control. Motor controllers from Quicksilver Controls (left) and Elmo Motion Control (right) provide supervision and implement motion-control strategies that optimize performance and minimize errors.

FEEDBACK LOOP

"I'm glad someone finally understands the outsourcing issue and the long-term impact to our economy. Our high-tech bigwigs are mortgaging our country's future, and they don't seem to care. They are like a bunch of lemmings—everyone else is doing it, so we have to do it. This is what happens when you let business people run high-tech companies.

Warren Peluso, in *EDN*'s Feedback Loop at www.edn.com/article/CA601510. Add your comments.

IS YOUR CURRENT FPGA DESIGN SOLUTION HOLDING YOU BACK?

FPGA Design | Ever feel tied down because your tools didn't support the FPGAs you needed? Ever spend your weekend learning yet another design tool? Maybe it's time you switch to a truly vendor independent FPGA design flow. One that enables you to create the best designs in any FPGA. Mentor's full-featured solution combines design creation, verification, and synthesis into a vendor-neutral, front-to-back FPGA design environment. Only Mentor can offer a comprehensive flow that improves productivity, reduces cost and allows for complete flexibility, enabling you to always choose the right technology for your design. To learn more go to **mentor.com/techpapers** or call us at **800.547.3000.**

DESIGN FOR MANUFACTURING + INTEGRATED SYSTEM DESIGN
ELECTRONIC SYSTEM LEVEL DESIGN + FUNCTIONAL VERIFICATION

Mentor Graphics®

THE EDA TECHNOLOGY LEADER

Tools support hot-swap and rewind debugging

The Platinum Edition of Texas Instruments' CCStudio (Code Composer Studio) integrated development environment introduces target-board hot-swap and a debugging-rewind feature that can help developers save time when tracking down system bugs. The new connect/disconnect feature allows developers to avoid a reset-and-reload sequence with the CCStudio tool set when hot-swapping target boards during a debugging session. This feature is useful when developers are simultaneously debugging hardware and software. A developer can replace a suspicious board with a known good board during the debugging session and eliminate the suspicious hardware or software as the source of potential errors. The connect/disconnect feature can save minutes between each reset-and-restart sequence.

The CCStudio Platinum Edition also introduces a rewind feature that allows developers to move both forward and backward within their source code during simulation. This feature allows developers to use a back-step keystroke and avoid reloading and stepping through a program from the beginning to find code errors. The rewind feature maintains a history of execution that normal step-and-run commands make so that a developer can view the program state and run code from earlier points in the program. The feature has no associated overhead, so it doesn't slow down the simulation as it records execution of the application.

Other enhancements to the CCStudio Platinum Edition include support for the CodeWright Editor; tuning tools and compiler upgrades that support all of the TI platforms; and a component manager that enables developers to manage upgrading and locking versions of the IDE components, including compiler and DSP/BIOS software-kernel versions. The CCStudio Platinum Edition now supports development for multiple TI platforms within a single tool installation, and the price for supporting all of the TI platforms is the same as the cost to support a single platform in earlier versions of CCStudio. The CCStudio Plat-inum Edition IDE is available now for $3600; includes 15 months of update-subscription service; and supports all TI platforms, including the TMS320C6000 DSP, TMS320C5000 DSP, TMS320C2000 DSP, and OMAP (Open Multimedia Applications Platform). There is also a free 120-day evaluation version available on CD-ROM.**—by Robert Cravotta**

▷**Texas Instruments**, www.ti.com/ccstudioplatinumpr.

Brushed, brushless motors serve tailored applications

Considerable segmentation exists in IC taxonomy, and it's easy to think that the motor world is less fragmented, but that idea is a misconception. Among the major motor categories are brushless units, and a new series of axial air-gap units from Applimotion features low weight, zero cogging, and a low-profile package. Applications include microliter metering in precision instrumentation, scanning equipment, and inspection systems. The motors feature diameters as large as 300 mm and axial thickness of 5 mm. The units operate from 5 to 48V supplies with standard three-phase brushless controllers. The frameless construction lets engineers slip these units into designs that currently lack internal motors. Prices range from $250 to $750, depending on size.

Voice-coil motors offer linear motion over a modest distance but at high speed. Members of the VM-series from Gee Plus produce peak forces from 12N (2.7 lbs) to 150N (31.5 lbs) for the VM8054. That largest unit has a 3.15-in. outside diameter and is 2.13 in. long. The overall stroke is 1.26 in. at 10% duty cycle and with a 500W input. The smallest member, the VM4632, has a 0.4-in. stroke, a 210W input, and a 10% duty cycle; it sells for $208.

For applications requiring miniaturization—a major factor in today's squeezed systems—the HG16 series of integrated, brushed dc motors from Nidec Copal may fill the bill. Each device includes a gear train, and an encoder measures 16 mm in diameter and 62.4 mm long. Targeting use in medical-lab equipment; small-camera pan, zoom, and tilt units; and compact printers, the series includes a dozen models with operating voltages of 6, 12, and 24V and gear ratios of 30-, 60-, 120-, and 240-to-1. Rated torque is 3.47 oz-in. for the 30-to-1 unit to 6.94 oz-in. for the 240-to-1 version. No-load speeds are 60 to 390 rpm, depending on gear ratio. Prices begin at $27 (100).

—by Bill Schweber

▷**Applimotion Inc**, www.applimotion.com.

▷**Gee Plus Inc**, www.geeplus.biz.

▷**Nidec Copal USA Corp**, www.copal-usa.com.

Take your motion, brushed or not, with a flat, axial air-gap unit from Applimotion (left), a voice-coil unit from Gee Plus (center), or an integrated dc motor with a gear train and an encoder in a narrow total package from Nidec Copal (right).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GLOBAL DESIGNER

ARM boosts support to Indian design shops

With ARM microprocessor cores becoming increasingly popular with Indian design houses, the Indian subsidiary of the company is stepping up its involvement in the local market. "We work directly with 50 companies, and the number is poised to grow with the introduction of technologies and tools. Nearly 2000 engineers in Bangalore and about 5000 across the country work with ARM architecture," says Atul Arora, president of the Commercial Operations-India Division of ARM Embedded Technologies Ltd.

Developers are designing ARM chips into home-electronics products, such as digital TVs and set-top boxes; mobile devices, including phones and PDAs; enterprise applications, including data-storage units, printers, and wireless LANs; and embedded systems for automotive, medical, and industrial applications. "ARM is looking to increase its partnership with Indian companies, and the ADC (ARM-Approved Design Center) program is another way to work with the local market," says Arora. ARM has four such centers in India, and a total of 11 in the Asia Pacific.

Wipro (www.wipro.com) has been working with ARM technology since 1997 and became an ADC member in 1999. Today, Wipro has a team of more than 250 ARM experts and has developed more than 50 ARM-based systems on chips, covering ARM7, 9, and 11 series using both third-party- and in-house-developed platforms. "The ADC agreement provides Wipro with early access to the entire ARM environment, enabling us to provide first-time-right designs," says A Vasudevan, vice president of the VLSI Group of Wipro Technologies.

A more recent inductee into the ADC program is MindTree Consulting (www.mindtree.com). The company has for more than three years been involved in ARM-based designs for a number of international customers. "To support our product-realization services, we decided to combine our domain knowledge and design expertise with ARM processors to expand our offerings to customers," comments SN Padmanabhan, vice president of R&D services at the company. The company is working on multiple ASSP (application-specific-standard-product) designs for customers.

–by Chitra Giridhar, *EDN Asia*

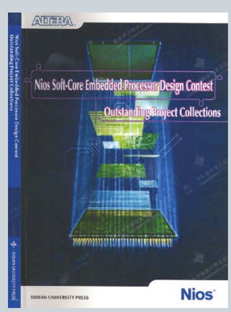
▷**ARM**, www.arm.com.

Asian SOPC-design applications now textbook cases

A low-cost DVB (digital-video-broadcasting) code-stream-monitoring system, an affordable articulation-type robot for industrial applications, and a real-time-face-recognition biometric system won first prizes at the recent Altera Nios Soft-Core Embedded Processor Design Contest among university-level design teams from China, Taiwan, and India. The contest has helped thousands of young Asian engineers to gain hands-on SOPC (system-on-programmable-chip)-design expertise. The company launched the contest in late 2004 and completed it in March 2005. More than 200 design teams from major Asian universities participated.

Altera has now collected all the finalist entries to the contest and published them in *Nios Soft-Core Embedded Design Contest* (Xidian University Press, ISBN 7-5606-1496-5/TN.0297, www.xidian.edu.cn). The book details a common theme through the finalists' designs: the ability to extract the best from Altera's FPGA flexibility and the customizable instructions of the Nios processor. China's winning entry, the DVB-code-stream-monitoring system by Xidian University (Shaanxi, China), uses Cypress Semiconductor's (www.cypress.com) CY7B923 to process DVB-ASI (asynchronous-serial-interface) signals. Then, using Altera's FPGA and Nios processor, the Chinese team designed a low-cost, compact DVB-code-stream monitor.

The face-recognition-biometric-design winning entry from the Indian Institute of Technology (Madras, India) implemented the entire design with Altera's SOPC and its custom-instruction feature using the Nios processor. The Taiwanese winning entry, an articulation-type robot from Southern Taiwan University of Technology, implemented a mechanical-arm servo-control system that the team based on Altera's FPGA and Nios processor.



The *Nios Soft-Core Embedded Design Contest* book includes design entries from finalists in the contest.

The Nios Design Contest 2004 was a success because of the diversity of creative applications from the entrants, according to Paul Chan, product manager for Altera's Asia-Pacific region. "We have seen Nios in applications such as robots, GPS (global positioning systems), MP3 players, DVB-S baseband processing systems, and fingerprint scanners," he says. Chan says the design contest has helped to create an awareness of the use of soft-processor and FPGA among budding designers. Judging the winning designs was difficult. Altera appointed a panel of engineering experts to judge them according to parameters such as technical difficulty, efficiency of coding, creativity, quality of hardware implementation, and practical significance.

The contest has wider implications because, says Chan, "Asian engineers' logic-design and embedded-processor-design skills are high-quality. As Asian companies expand into the global market, creativity and innovation will be crucial in developing a sustainable competitive advantage, and the results of the Nios-design contest show a positive signal of this trend."**–by NS Manjunath, *EDN Asia***

▶**Altera**, www.altera.com.

The thermoelectric-cooler device includes a cooling fan, heat sink, six thermocouples, and heat-sink compound to carefully control glass-surface temperature.

RESEARCH UPDATE

BY BILL SCHWEBER

Noninvasive technique measures humidity in sealed glass case

The National Aeronautics and Space Administration's Langley Research Center has designed a technique for continuously measuring the humidity within the glass cases holding the original US Declaration of Independence, Constitution, and Bill of Rights. The noninvasive approach provides real-time assessment using the well-established chilled-mirror-hygrometer method of observing the formation of condensed water droplets inside the glass. However, this technique adds extra attention to detail and established calibration factors to correct for errors and offsets when determining the precise dew point.

An aluminum-plate heat sink attaches to the glass, and a thermoelectric module and integral fan cool the plate. An array of six thermocouples within the plate measures the temperature of the cooled outer surface of the glass panel; heat-sink compound between the thermocouples and the glass ensures low thermal impedance. As the thermoelectric module's output temperature ratchets down in small increments, an observer looks at the glass with a flashlight and magnifying glass for condensation to form the first water droplets on the glass's inner surface. Researchers then apply adjustment algorithms, along with data sets they collected in equivalent lab setups, to determine the internal humidity and dew-point values.

You can find a summary of the research at the June 2005 issue of www.techbriefs.com and a full report at http://techreports.larc.nasa.gov/ltrs/PDF/2004/mtg/NASA-2004-ncsl-cgb.pdf.

▷**National Aeronautics and Space Administration**, www.nasa.gov.

Mobile-phone fuel cell triples capacity

Fujitsu Laboratories in conjunction with NTT DoCoMo (www.nttdocomo.com) has shown a prototype of a micro-sized fuel cell with 18-cc capacity and an external charger that uses methanol at 99% concentration, far higher than the 30% conventional concentration. In passive-cell designs, the higher methanol concentration soon overwhelms and stops the cell operation due to a saturation-and-permeation phenomenon, even though it offers more potential capacity. Fujitsu used a new membrane material, which significantly reduces this methanol-crossover effect.

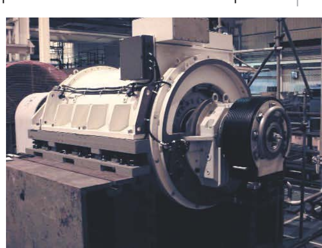
The prototype cell weighs 190g and measures 150×56×9 mm. Its maximum power-generation rating is 9W, and it can charge a trio of lithium-ion cells at 5.4V/700 mA.

▷**Fujitsu Laboratories**, www.labs.fujitsu.com.

PHOTONIC RADIO GETS CLOSER

The DARPA (Defense Advanced Research Projects Agency) has awarded a contract to Phasebridge Inc to further the development of an optical RF QPSK (quadrature-phase-shift-keying)-modulation technique for use in ultrawideband, frequency-agile, military-radio systems. The project's goal is to integrate frequency-synthesis and conversion methods for microwave through millimeter-wave channel frequencies. This objective requires electro-optical conversion, using integrated optics and micro-optical lenses, which are low-cost, lightweight, and precisely aligned with minimal production trim.

▶**Phasebridge**, www.phasebridge.com.



Serious superconducting motor gets real

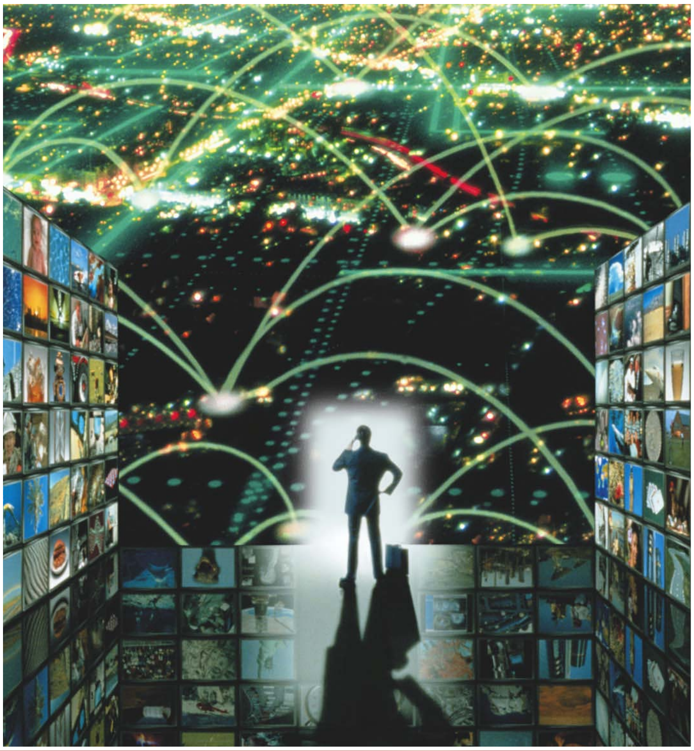
A 5-MW motor using HTS (high-temperature-superconducting) wire and magnets has passed load- and ship-mission-testing protocols. American Superconductor designed the motor under an Office of Naval Research contract as an interim step toward a 36-MW, 49,000-hp, 120-rpm unit under development for ship propulsion. The goal is a propulsion system that has one-third the weight and one-half the size of conventional copper-based motors of the same rating.

The 5-MW motor underwent static and dynamic tests at the Center for Advanced Power Systems at Florida State University (Tallahassee). Alstom Power Conversion's (www.powerconv.alstom.com) Rugby, UK, facility designed, built, and conducted further tests on the stator- and marine-drive electronics. In the static tests, the motor ran at full load and speed, 230 rpm, for 21 hours; resultant temperature and performance data agreed with design predictions. In the dynamic test, the test station imposed load variations of 0.5 to 10% around moderate- and full-power operating points. Testing also used hardware-in-the-loop simulation to control the motor and emulate complete propulsion-system operation.

▶**American Superconductor, www.amsuper.com.**

08.18.05

VIDEO AND VOICE ANYWHERE, ANY TIME, TO ANY DEVICE.



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	Infrastructure		Handsets/Terminals			
	MSC81XX (Channel Density 24-336)	MSC711X (Channel Density 4-48)	MXC	i.MX21 (MX938MX21)	i.MXL (MC9328MXL)	MCF52XX
High-Density Gateway	● Carrier Class					
Media Access Gateway	● Enterprise					
IP PBX	● Enterprise	● Enterprise				
Gateways & IADs	● Residential/SOHO	● Residential/SOHO				
Video Conf/Transcoding	● Enterprise					
Wireless Transcoding	● Enterprise					
Video Transcoding	● Enterprise					
Terminal Adaptor		● Residential/SOHO				● Residential/SOHO
Switch/Router						● Enterprise
Home Gateway Triple Play			▲ Desktop/Set-top			
V2IP Phone/TV Out			▲ Desktop/Set-top	▲ Desktop/Set-top ▲ Wifi Handsets		
VoIP Phone				▲ Desktop/Set-top ▲ Wifi Handsets	▲ Desktop/Set-top ▲ Wifi Handsets	▲ Desktop/Set-top ▲ Wifi Handsets ● Residential/SOHO
IP Camera				▲ Video Surveillance		▲ Video Surveillance ● Residential/SOHO
Video Doorbell				▲ Video Surveillance	▲ Video Surveillance	▲ Video Surveillance ● Residential/SOHO

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BY HOWARD JOHNSON, PhD

Millions and billions

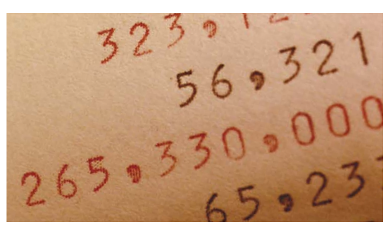
Did the US Congress appropriate $94 million, or was it $94 billion, for the Department of Agriculture in 2005? Who can remember? To most people, all big numbers sound the same, so they care little about the difference. Besides, if the amount ever causes a problem, Congress can always legislate a bigger debt ceiling to work its way out of difficulties.

A similar psychological effect pervades the world of tiny numbers—humans amalgamate all diminutive quantities into a single concept of "small." I regularly observe this effect when asking an engineer, "What is the rise time of your signals?" Clearly, the answer is *small*, but when put on the spot, some people are unsure whether the measurement of this rise time is in picoseconds, nanoseconds, or microseconds. Do you know the exact value of your rise time? I cannot imagine any more important question with which to begin the analysis of electrical-circuit behavior.

The ratio of signal rise time to physical delay in an electrical circuit determines how the circuit behaves. A small ratio, meaning a short rise time compared with the innate time delay of the circuit, produces distributed behavior. The other possibility, a large ratio, invokes lumped-element behavior. In both cases, the *relative* comparison of the rise time with the physical extent of the circuit determines behavior, not the absolute value of either quantity.

You need to know whether your circuit is distributed or lumped, because distributed systems sometimes display wiggly, undulating waveforms. They respond differently at different points and may exhibit severe resonances. On the other hand, lumped-element circuits more often work in an easily understood manner. You can describe lumped-element circuits using simple circuit schematics, and you can quickly simulate them in Spice.

For example, consider a thick FR-4 backplane with press-fit connectors. The vias in this design have a barrel diameter of 0.035 in. and a length as great as 0.250 in. You can calculate the raw, unloaded circuit delay for signals moving through such vias as ($\frac{1}{4}$ in. length)×(180 psec/in.)=45 psec.



To most people, all big numbers sound the same.

In an old 33-MHz backplane-transceiver application (that is, BTL/Futurebus), assuming rise and fall times of 2 nsec, the ratio of rise time to via delay is inconsequential. At such a slow speed, you can model these backplane vias as simple lumped-element devices—usually shunt capacitances. In addition, because the via capacitances are not very great (2 pF), such vias work fine on a 33-MHz bus with 2-nsec rise and fall times.

A serial application running at 10 Gbps presents an entirely different story. The bits in this application fly by *300 times faster*, with correspondingly smaller rise and fall times. A factor of 300 is *huge*. In such a fast system, a via delay of 45 psec can easily exceed the signal rise time. Thick backplane vias at this speed respond in a highly distributed fashion and can become significant problems.

When considering any aspect of your circuit geometry, the relation between physical size and rise time helps determine the relative importance of that object in the overall scheme of the circuit.

If you are uncomfortable exercising your judgment about which circuit features might matter at high speeds, try translating your gut experience at low speeds into the high-speed domain with a simple analogy. Ask yourself whether it would be reasonable to solder a 75-in.-long metal cylinder onto each of your 33-MHz bus traces. Sound ridiculous? Yes. Precisely as ridiculous, according to the laws of physics, as placing a 0.25-in. via on a 10-Gbps serial link.

Digital design, unlike politics, requires strict adherence to the laws of physics—immutable laws that you cannot legislate out of existence. EDN

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

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Analog Applications Journal

BRIEF

Simple DSP interface for ADS784x/834x ADCs

By Tom Hendrick • *Component Applications, Data Acquisition Products*

The 12-bit ADS7841 and 16-bit ADS8341/3 are pin-compatible, 4-channel analog-to-digital converters (ADCs) with a synchronous serial interface. Typical power dissipation is 2 mW at a 200-kHz throughput rate on the ADS7841 and 8 mW at 100 kHz on the ADS8341/3. The 12-bit ADS7844 and 16-bit ADS8344 are pin-compatible, 8-channel ADCs with the same typical power requirements as their 4-channel cousins.

The low power, high-speed, and onboard multiplexer of these devices make them ideal for battery-operated systems such as personal digital assistants, portable multichannel data loggers, and measurement equipment. The datasheets for these devices show various ways to interface the parts to microcontrollers with a serial peripheral interface (SPI), but they do not mention how to use these parts with high-performance digital signal processors (DSPs). This article provides an easy way to connect these parts with any Texas Instruments (TI) DSP that contains at least one multichannel buffered serial port (McBSP). The information here pertains to the TMS320F2812 and all devices in the TMS320C5000™ and TMS320C6000™ DSP platforms.

Digital Interface for Microcontrollers

The digital interface section of the datasheet for all five of these devices shows a typical SPI with burst clock mode of operation based on 8 or 16 clock cycles. While an SPI interface is certainly not difficult to implement, there can be a bit of difficulty associated with getting the received data into a format that the processor can actually use. Figure 1 shows a typical 8-bit SPI interface.

The difficulty many users run into with this interface is in formatting return data with minimal software overhead. At first glance, it is not always obvious to new users of these parts that the most significant bit (MSB) is presented on the 9th clock cycle. With a microcontroller like the MSP430 series of devices and the SPI interface shown in Figure 1, the 7 MSBs of data are stored in an 8-bit register, with the 5 least significant bits (LSBs) stored in a second 8-bit register. In order to store the converted data in a meaningful fashion, both the upper and lower bytes would need to be shifted (left or right) and then concatenated before being stored into a data array for future processing. In applications such as motor control, the software latency of these data manipulations proves too costly.

The process can be simplified a little if the microcontroller is capable of running with a 16-bit SPI interface, such as the TMS470 series of devices from TI. For the 12-bit parts, all returned data can be captured in a single 16-cycle transmission. To accomplish this, simply shift the command byte to the left by 7 bits as shown in Figure 2. The SPISCS line shown in Figure 2 could be tied to the chip select line of the ADC if multiple devices share the SPI bus.

The modified 16-clock SPI interface of Figure 2 sends the BUSY signal high on the falling edge of the 15th clock. In some applications, this approach might still require a data shift. The 12-bit data is MSB-aligned and the MSB is provided twice. The software overhead becomes less of an issue in this case since the shift can be done during the actual data reception in the SPI routine.

Figure 1. Typical 8-bit SPI interface

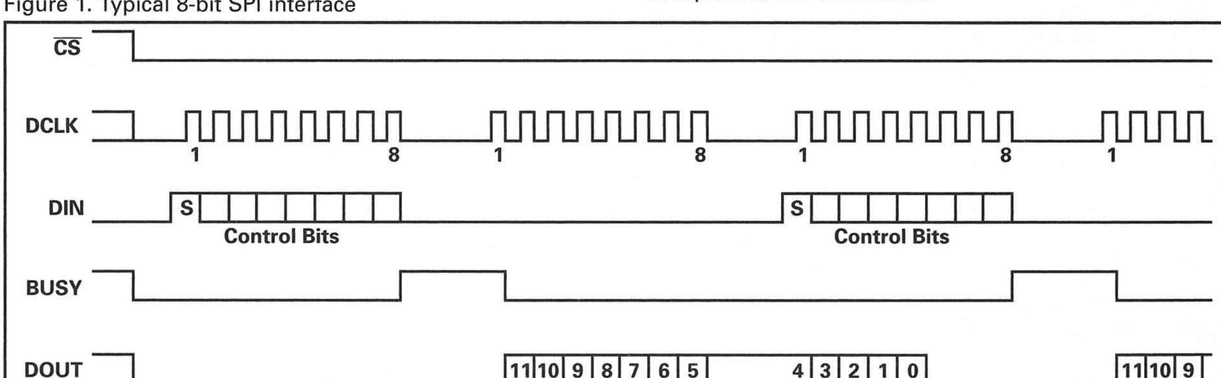


Figure 2. Modified 16-clock SPI interface

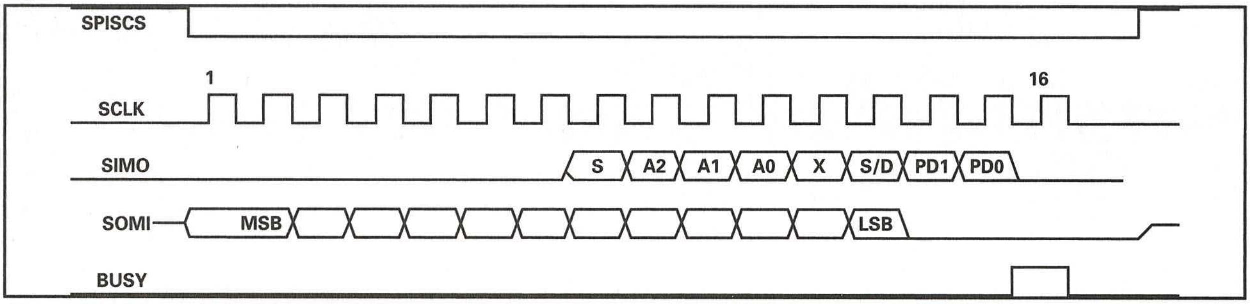
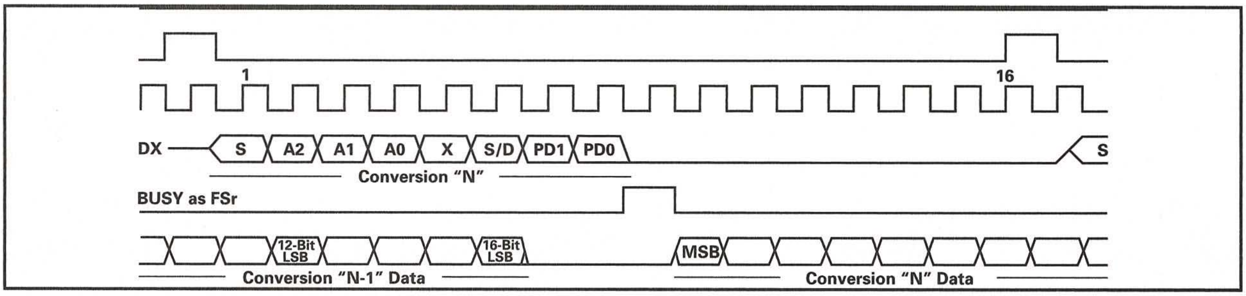


Figure 3. DSP transfer with 16 clock cycles



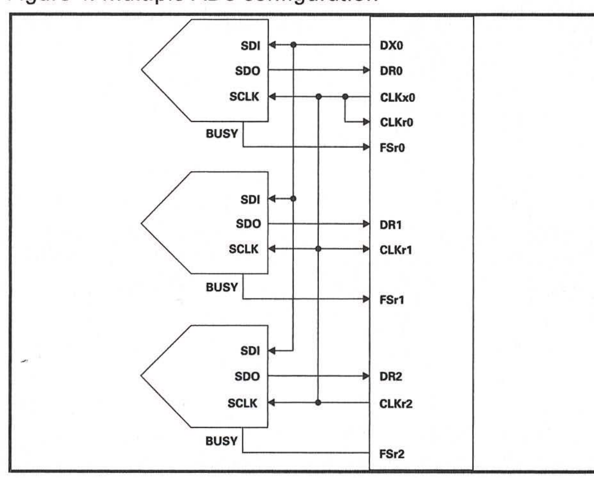
There are two drawbacks to this approach—first, the LSB is lost. The LSB is cut short during the switch from sample to hold mode and the host processor will always read it as a "one." The second issue is latency. These converters enter their acquisition phase after the A0 bit is read into the part. The data shown in Figure 2 would be the conversion results from the previous cycle, which adds latency to the system. When the 16-bit parts are used, the problem is aggravated even further. An 8- or 16-bit SPI device like the MSP430 or TMS470 would need to issue at least 24 SCLKs to complete a 15-bit transfer. If the entire 16 bits of data are needed, a total of 32 clocks would be required. Data manipulation would still need to be done, adding software overhead.

Digital interface for TI DSPs

Using the high speed and flexible capabilities of the McBSP ports found on the TMS320F2812 or the C5000™ and C6000™ DSP platforms can virtually eliminate the software overhead associated with the microcontroller and the SPI interface.

The McBSP ports have independent transmitter and receiver functions. Since transmit and receive sections are independent, transmit and receive frame sync (FS) signals are also independent. If the chip select (/CS) signal is tied low, the BUSY signal can be used as the frame sync return (FSr) to indicate that a serial stream is on its way into the receiver. The data transfer to the DSP is done without any further need for manipulation. Setting the data transfer length in the DSP to 16 bits allows exactly the same software routine to be used with the 12-bit ADS7841 or the 16-bit ADS834x devices. As shown in Figure 3, the output data is actually wrapped between conversion start commands so that there is minimal latency between conversion cycles. Data is presented to the DSP MSB first from both the 12-bit and 16-bit devices. If LSB alignment is required, a 4-bit shift could be implemented to the received data as it is sampled. Another added advantage of using the DSP is the possibility to realize simultaneous sampling on up to three devices on a DSP with multiple serial ports. This would be done by using a single "master" transmitter tied to all three ADCs and returning the master clock to all three "slave" receiver ports. The BUSY signal from each of the three ADCs would again act as the FSr to each receiver. Figure 4 shows a potential method for implementing multiple ADCs in a simultaneous sampling application.

Figure 4. Multiple ADC configuration



Conclusion

The ADS784x/ADS834x data converters are truly versatile with their simple serial interface, low power, high-speed operation, and ease of use. They are ideal for portable and handheld applications that require excellent performance capability and upgrade flexibility. For additional information on the devices mentioned in this article, please contact your local distributor, the TI Product Information Center listed below or the Data Converter Applications team at dataconvapps@list.ti.com

Related Web Sites

dataconverter.ti.com
dsp.ti.com
microcontroller.ti.com
www.ti.com/device/partnumber
Replace partnumber with ADS7841, ADS7844, ADS8341, ADS8343, ADS8344 or TMS320F2812

RACE TO RoHS

FROM TI STANDARD LINEAR AND LOGIC

ARE YOU READY FOR RoHS?

***R**eliable, **O**bservant, **H**elpful, and **S**traightforward Compliant Solutions from TI.*

Will you be ready when the European Parliament's directive on the restriction of hazardous substances (RoHS) kicks in in July 2006? The directive mandates that electronic devices sold in the EU after that date be certifiably free of lead and certain other elements traditionally used in electrical and electronic equipment. Japan, China, and other nations are expected to follow the EU's example, so the clock is ticking toward the day when the world-wide electronics market will be lead (Pb)-Free.

The looming directive has implications for engineers, managers, and procurement specialists throughout the electronics industry. While other electronics manufacturers scramble to engineer alternatives to existing components, Texas Instruments (TI) has been producing Pb-Free electronics since 1989. "We saw it in the very beginning as a competitive advantage," says Jan H. Pape, marketing director of TI's Worldwide Standard Linear and Logic (SLL) group. "As it turns out, our Pb-Free definition is equal to or better than the RoHS definition."

As of today, 95% of TI's Standard Linear and Logic products conform to the RoHS directive (the remaining 5% service military, medical, and certain industries temporarily exempt from RoHS). Moreover, TI's nickel-palladium-gold (NiPdAu) answer to the Pb-Free solder problem is backward-compatible with existing reflow soldering processes and is free from the whisker-artifact problems associated with alternatives like matted tin.

"If you go to pure tin, you actually have to increase the reflow solder temperature to achieve the same reliable solder contacts," says Pape. "It adds to costs—logistics, MRP (manufacturing resource planning), inventory positions, the whole thing. Over the last 16 years, we've shipped over 30 million Pb-Free units, confirming that NiPdAu is a reliable finish."

As the RoHS deadline approaches, customer support for the transition to Pb-Free manufacturing has become a critical issue. Surveys show that only half the industry is aware of and preparing for Pb-Free conversion. The fear is that the other half, once it's convinced that it will have to convert, will create a supply squeeze for NiPdAu in its rush to do so.

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Part numbers themselves have become a source of confusion as change-over to RoHS compliance nears. To simplify matters, TI has introduced alternate part numbers for existing components, adding JEDEC-standard codes to indicate their status. For example, an LM358DR, a RoHS-compliant Pb-Free op amp, would add an "E" for RoHS compliance and a "4" for the NiPdAu plating. If it had already been converted to Green compliance, then the suffix would be "G4" (e.g., legacy P/N LM358DR, unique P/N LM358DRG4).

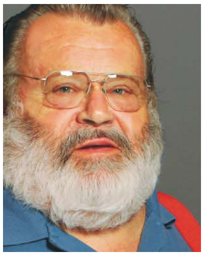
Customers planning ahead can search for Pb-Free components at TI's website, www.ti.com/productcontent, where they can look up a single part or enter a bill of materials (BOM) list for up to 1,000 separate part numbers to check their Pb-Free status. The company also provides a BOM-crossing tool and customer-support team that will accept competitor's part numbers and return a list of RoHS "Gold" compliant TI alternatives, usually within 48 hours.

RoHS Gold is a TI term used to show full compliance to the industry RoHS requirements, with additional customer advantages. These advantages include:

- TI's primary Pb-Free Solution, Nickel Palladium Gold (NiPdAu) is "Whisker-Free."
- TI is adding unique Pb-Free Part Numbers.
- TI has more than 15 years experience with NiPd based leadframes.
- TI is doing 4 conversions (Pb-Free, Whisker-Free, High-Temp, & Green) at the same time for most parts resulting in fewer changes for customers.
- TI provides easy access to key Pb-Free information.

While the industry expects that the closure on the Green definition will not happen before 2009, TI is already well on its way to bringing its entire line into Green compliance.

"We were ahead of the industry in going to Pb-Free, we are preparing to go to Green now from a TI point of view," says Pape. "It's our tradition to set the industry standard. Customers can feel safe in knowing that TI is the reliable Pb-Free supplier during this time of uncertainty."



BY RON MANCINI

Compare Spice-model performance

I wanted to use Spice to predict the PSRR (power-supply-rejection-ratio) performance of an op amp. My plan was to evaluate the effects of adding decoupling capacitors or local power-supply filtering to improve the circuit's PSRR, but first I needed to establish a baseline-PSRR performance. I inserted an ac signal into the ground return to check the OPA132's PSRR performance, and the results were terrible; the plot indicated that the OPA132 has 8-dB PSRR capability. This op amp's data sheet indicates a PSRR of 100 dB at 90 Hz. Because of the difference between the model and the data-sheet performance, I was side-tracked into looking at Spice models rather than improving PSRR.

I can't think of anything more objectionable than looking into the innards of software; thus, I enlisted the help of Neil Albaugh, an expert in analog circuits and Spice. Neil confirmed the poor PSRR performance of the OPA-132 model, and he calmed my whining about the poor models with which design engineers have to work. He checked out the measurement circuit by analyzing an OPA227, and he received excellent PSRR performance. The semiconductor industry generated early Spice models by running PSpice Parts simulation software. This program generates a standard Boyle-op-amp model from extracted device parameters (**Reference 1**). The basic Boyle model does not model the following parameters: input-offset voltage and current; input current and voltage noise; input protection, impedance, or capacitance; output-current flow from the power supply; quiescent-current changes with power-supply-voltage or temperature changes; gain versus temperature; CMRR (common-mode rejection ratio) or PSRR versus frequency; and PSRR.

The latest generation of macromodels is considerably better than their predecessors.

The enhanced-Boyle model follows the basic-Boyle model and adds the following parameters: input voltage and current noise, input capacitance and impedance, quiescent-current changes with power-supply voltage, and output-current flow from the power supply. These additions make the enhanced-Boyle model much more usable, but you can't do an in-depth analysis with these poor models.

The latest generation of macromodels is considerably better than their predecessors. The OPA227 performs excellently in the PSRR test; it is a late-generation model with the latest features. When you first get a model, try to open it with a text editor, such as Microsoft Wordpad, to see what the model contains. Older op-amp models may be Boyle or enhanced-Boyle models that have few features. A newer op amp, such as the OPA301, has an improved model and opens with the statement "OPA301.MOD." The descriptive data within the OPA301 model reads: "Model temperature range is −40°C to +125°C, not all parameters accurately track those of an actual OPA301 over the full temperature range but are as close as possible." This model offers 20 features, such as PSRR versus frequency, for this op amp. This scenario is still imperfect, but semiconductor manufacturers are coming close.

Reference 2 is a good source for older models. It gives the history of a company's experience with making macromodels, and it contains a wealth of useful information. The newer models contain descriptions that you can access. Knowing your model is a key to success when you use an analysis program. Coupling the model knowledge to model testing, correlating the model to the data sheet, and correlating the model to lab testing are the required series of events to ride the road to analysis success. EDN

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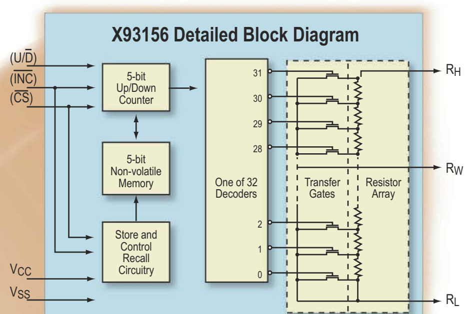

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Key Parameters

Description	Conditions	MIN	TYP	MAX	Unit
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	X93155	4.5	5	5.5	V
	X93156	2.7	-	5.5	V
End-to-end Resistence		35	50	65	kΩ
R_H, R_L Terminal Voltages		0	-	V_{CC}	V
Power Rating	R_{TOTAL} = 50 KΩ	-	-	1	Mw
Noise	Ref: 1kHz	-	-120	-	dBV
Wiper Resistance	X93156	-	-	1100	Ω
Wiper Current		-	-	0.6	mA
Resolution		-	3	-	%
Temperature (Industrial)		-40°C	-	+85°C	C

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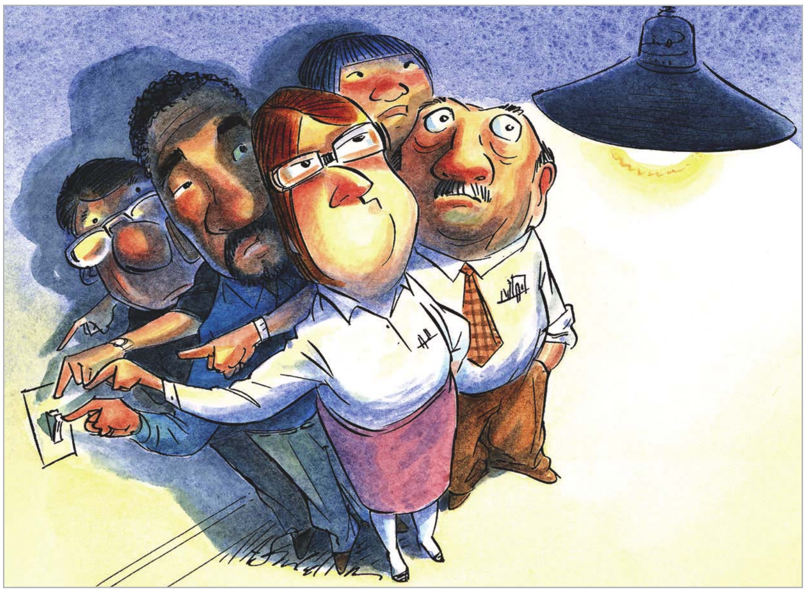
Shedding light on radiation testing



DANIEL VASCONCELLOS

We recently designed a 2-kW, more-than-93%-efficient power converter for a manned space application. The design uses the latest generation of 500 and 200V power MOSFETs, which are available as commercial encapsulated plastic parts, for both converter-drive and synchronous rectification. For several reasons, including cost, schedule, volume, weight, and—most important—ease of connection, we opted to use the FETs in this form, rather than purchase die and have them mounted in hermetic headers—thereby making them "special" parts. We devised a set of screening tests and procured parts for sample testing. The parts did well in parametric testing over the full military-temperature range, even though they weren't specified for it. They also met all of the DPA (destructive-physical-analysis), outgassing, and other materials requirements. The only additional set of tests required was radiation-susceptibility testing.

The program preference was for heavy-ion testing, so that's what we did. Because heavy ions do not readily penetrate the encapsulant, it was necessary to subject the radiation-test articles to a plastic stripping process to expose the die. After successfully completing the stripping process, we subjected the parts to room-temperature parametric tests; they passed. We developed test fixtures that use high-value resistors in the drain circuit, pulled up to an adjustable power supply, and used a biasing circuit to apply the appropriate reverse bias on the gate, simulating the application's gate bias. During testing, the high value of drain resistance reduces both the available current and the destructive energy available during radiation-induced turn-ons of the parasitic bipolar within the FET structure, allowing the device to recover. In turn, we could sneak up on the drain potential at which these events first began to happen and record the frequency of these events versus drain voltage. To save time, we checked out the fixtures in parallel with the stripping of the actual test articles by using encapsulated parts. Our test engineer, who would conduct the testing, then shipped the test articles and the fixtures to the test site.

Shortly after testing was to have begun, our test engineer found that all of our test articles had excessive drain-to-source leakage before he had subjected them to any radiation! The parts had passed parametric tests at room temperature, based on data-sheet maximums, but no one had compared the measurements one-to-one with the test data collected on the same parts before stripping.

The need to considerably reduce the drain resistance to run the tests made more current and energy available, which limited the resolution of the sensitivity data. After the fact and after some head-scratching, we found the problem was due to room light impinging on the exposed FET die. The resulting photo current in the FET body diode drastically increased the measured saturated drain-to-source current. Turning off the lights could have solved the problem … and made the microammeter unreadable. (Whatever works!) EDN

Charles Clark, a member of EDN*'s Editorial Advisory Board, is a Technical Fellow at The Boeing Company.*

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We need a regular supply of "Tales," and who better than you, the loyal readers, to supply them? Send a narrative describing an especially sticky engineering problem that bedeviled you to Maury Wright at mgwright@edn.com. Tales should provide both compelling reading and a learning opportunity for our readers. (See previous examples on the Web at www.edn.com/article/CA608177 and CA624946.) If we publish your submission, we'll send you a $200 American Express gift check.

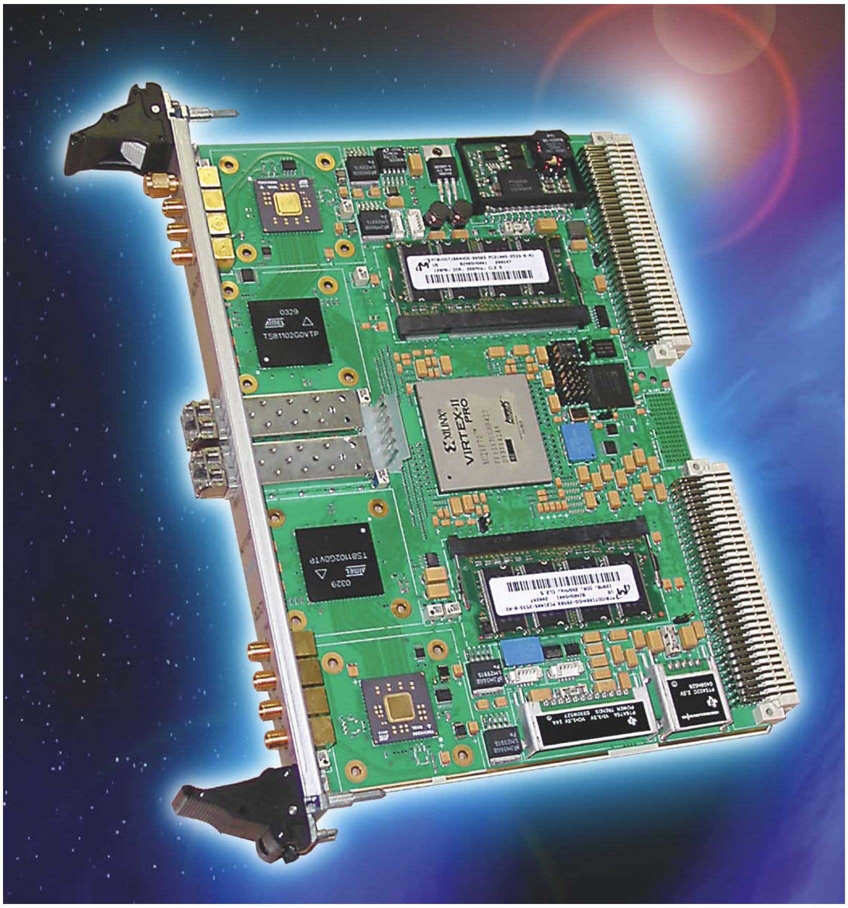

Figure 1 The VXS Quixilica Neptune combines FPGA technology with 2G-sample/sec ADCs for high-performance applications.

BY WARREN WEBB • TECHNICAL EDITOR

VME fosters a fabric future

WHILE NEWER EMBEDDED ARCHITECTURES VIE FOR HIGH-PERFORMANCE APPLICATIONS, VENERABLE VMEBUS VENDORS PEN A FABRIC-BASED STRATEGY FOR CONTINUED SURVIVAL AND FUTURE GROWTH.

Although the VMEbus (VERSAmodule Eurocard bus) has been the workhorse of the embedded-system industry for almost a quarter of a century, it has struggled to compete with newer, faster board standards. Saddled with a parallel, multidrop data bus and a commitment to compatibility with 20-year-old technology, VME has found a home in the long-life-cycle systems that military, industrial-computing, aerospace, and medical designs require. To update their image and expand market possibilities, board manufacturers have recently proposed a series of extensions to the base VMEbus specification that add new connectors and several flavors of high-speed serial datapaths.

Launched in the early 1980s, VMEbus employs a 3, 6, or 9U pc board with a pin-and-socket-connector interface to the backplane to withstand harsh industrial applications. The developers of the VMEbus created it by combining Motorola's VERSAbus electrical standard and the Eurocard mechanical form factor. Although VERSAbus has since faded away, VME became popular with designers because it was processor-independent, based on a reliable mechanical form factor, and released as a nonproprietary standard. The original standard, now called IEEE 1014, specifies a master-slave configuration with 40-Mbyte/sec asynchronous data transfers between boards based on a variable-speed handshaking protocol. A VME backplane can contain as many as 21 card slots with multiple master computer boards. Many VME boards that conform to this original specification are still in use today.

Although upgrades were inevitable, VME manufacturers agreed to maintain compatibility with legacy hardware to protect user investments. VME has undergone several upgrades to increase the shared-bus-data-transfer rate, but each allows older products to communicate at their original speed. VME64, which ANSI (American National Standards Institute) and VITA (VMEbus International Trade Association) approved in 1996 as ANSI/VITA 1.1, increased data rates to 80 MHz by doubling the path width to 64 bits. Another doubling of the data rate to 160 Mbytes/sec reduced the transfer protocol from a four-edge to a two-edge handshake. The 2eSST (two-edge source-synchronous-transfer) interconnect of ANSI/VITA 1.5 can transfer data across the VMEbus at 320 Mbytes/sec. Although these upgrades are compatible with earlier hardware, data transfers must occur at the slowest device rate.

In many applications, expected data rates exceed the limitations of any shared-bus system. In these high-speed applications, such as medical imaging and other signal-processing systems, designers have turned to auxiliary communications techniques to bypass the shared bus and transfer data directly between subsystems.

AT A GLANCE

- Stuck with a limited-data-rate parallel bus and legacy compatibility, VMEbus designers have shied away from high-performance applications.
- A series of performance updates has taken VME's parallel-bus data rates from the original 40 Mbytes/sec in 1981 to today's 320 Mbytes/sec.
- In its third decade, VME's serial-switched-fabric technology promises to extend its effectiveness to future embedded-system designs.
- The failure of the industry to adopt a single fabric technology and maintain legacy compatibility could reduce the appeal of VME for future designers.

VME has a history of third-party add-ons that use point-to-point connections and external crossbar switches to send high-speed information around the bandwidth-limited VMEbus (**Reference 1**). These point-to-point-communications schemes multiply their basic bandwidth by allowing several transfers to occur simultaneously. These early, high-speed-communications channels were the forerunners of today's switched-fabric interconnects.

FABRIC FEATURES

The main benefit of a switched fabric is that each connection is a direct point-to-point datapath, thereby eliminating the multiple connections of a parallel-bus structure. Most switched-fabric specifications call for LVDS (low-voltage differential signaling) for maximum bandwidth between nodes. Another obvious benefit of serial connections is the reduced connector sizes due to the use of fewer signal lines. A typical switching fabric may use several stages of high-bandwidth switches to route transactions between a source and a target. A sophisticated switched-fabric system can also increase system availability by routing data around defective paths or nodes.

Switched-fabric technology has become popular with embedded-system designers; however, a clear favorite and market leader has yet to emerge. CompactPCI and ATCA (Advanced Telecom Computing Architecture), two current board-level standards, do not call out the specific fabric technology for data transport. Instead, a series of subsidiary specifications defines backplane details for the various fabrics, such as Ethernet, InfiniBand, StarFabric, PCI Express, and RapidIO. To satisfy differing views within the industry, the VMEbus specification will also allow multiple fabric technologies at the risk of interoperability issues.

The VXS (VITA 41 Switched Serial Extensions) appends fabric technology to the VMEbus and preserves compatibility among products. The VXS specification defines a payload card; a switch card; and a new, high-bandwidth P0 backplane connector. It also retains the standard P1 and P2 parallel VMEbus connectors. Each P0 fabric port comprises two sets of four ganged serial-bit channels, one set for input data and the other set for output data. The specified P0 connector technology supports data rates as high as 10 Gbps for each serial channel. Payload cards are simply standard VMEbus processor, memory, or I/O boards with the addition of the new VXS-fabric interface. With no P1 and P2 connectors, switch cards have the same form factor as payload cards and include as many as 18 full-duplex serial connectors plus a power connector. The switch card contains the fabric switching necessary to route serial data between payload cards. To remain fabric-agnostic, VITA 41 subspecifications define switches and payload cards for InfiniBand, serial RapidIO, gigabit Ethernet, and PCI Express. David French, director of business development at SBS Technologies, says, "VXS evolves the VMEbus infrastructure and nurtures the VMEbus market. It offers a low-risk, evolutionary product-development path consistent with VME life-cycle advantages."

The VXS requires a special fabric-compatible backplane that supports two to 20 payload cards and one or more switch cards. A full-width backplane holds nine payload cards on each side and two switch cards occupying the two center slots for a total of 21 boards. With two switch cards, each payload card can connect to any other payload card through two redundant paths. Many fault-tolerant and high-availability applications require this dual redundancy. Hybricon offers a family of VXS backplanes with two switch-card slots and as many as 18 payload slots. The company constructs the boards in a 20-layer, low-noise stripline design with the outside layers incorporating a chassis ground-EMI shield and rigidity stiffeners every two slots. Hybricon tests the parallel-VMEbus portion of each board at speeds as high as 320 Mbytes/sec, as the VITA 1.5 2eSST standard requires. The company also offers 21-slot versions for the VITA 41.1 VXS InfiniBand Protocol Layer Standard and VITA 41.2 VXS Serial RapidIO Protocol Layer Standard. Custom configurations with fewer than 21 slots are also available.

Figure 2 The IB4X-V41-AC 24-port InfiniBand switch card from SBS Technologies routes switched serial interconnections over the standard VME backplane.

DATA CRUNCHER

Tek Microsystems and QinetiQ recently announced the Quixilica Neptune, a VXS-standard product that combines FPGA technology with dual-channel, 2G-sample/sec ADCs for signal-intelligence, radar, and electronic-warfare applications (**Figure 1**). A Xilinx Virtex-II Pro XC2VP70 FPGA is at the heart of the Neptune product and provides the interface between the ADCs, memories, and I/O resources on the card. Bill Smith, PhD, manager of the Real Time Embedded Systems Group at QinetiQ, says, "Developers can implement their front-end-signal-processing algorithms in the large, user-programmable FPGA on Neptune to reduce the amount of data that needs to be transferred offboard for subsequent processing." The Quixilica Neptune VXS-1 is available from Tek Microsystems; prices start at $31,000.

The IB4X-V41-AC from SBS Technologies is a 24-port 4× InfiniBand switch card in a VITA 41 form factor

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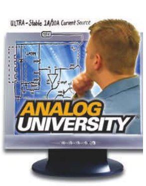
ADC08D500	8-Bit, dual, 500 MSPS (1 GSPS in DES mode)
ADC08D1000	8-Bit, dual, 1 GSPS (2 GSPS in DES mode)
ADC08D1500	8-Bit, dual, 1.5 GSPS (3 GSPS in DES mode)



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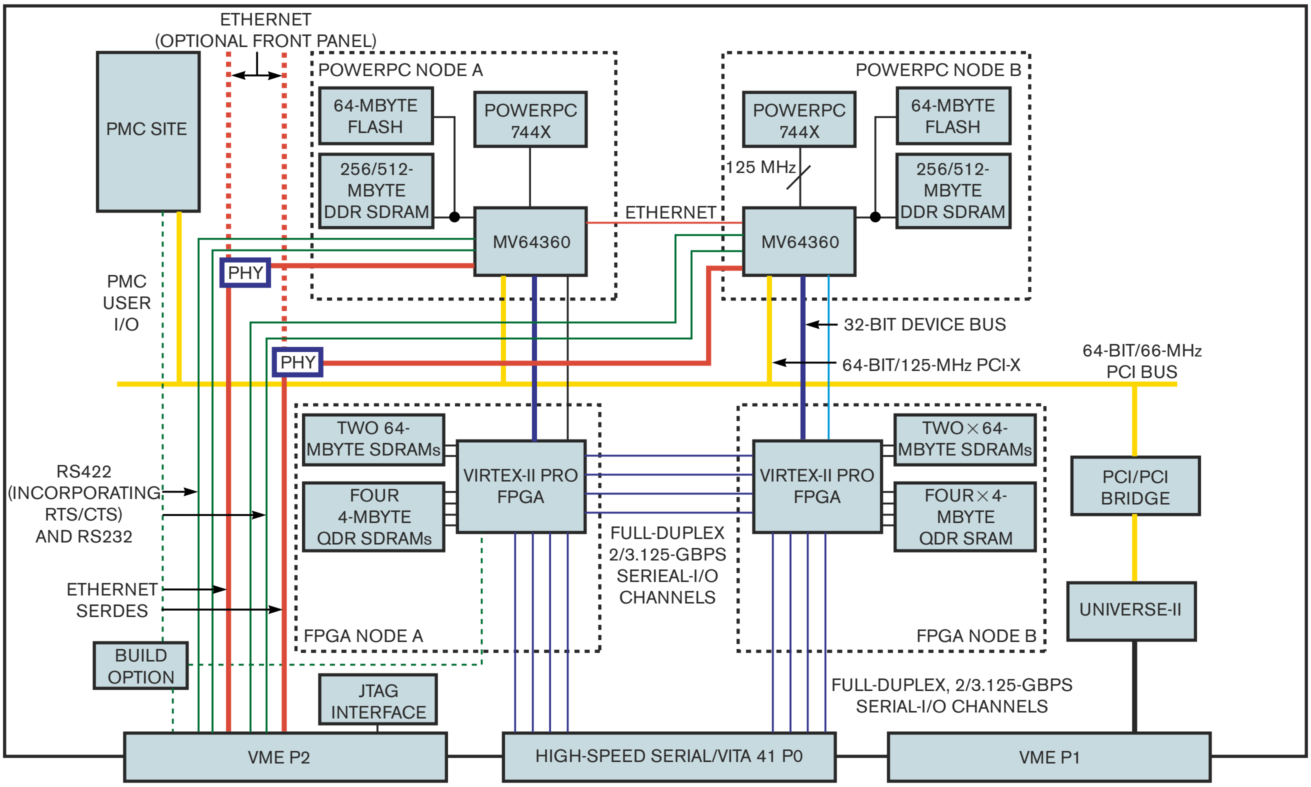

Figure 3 The VPF1 quad-signal-processing card from Vmetro provides dual PowerPC processors and FPGAs plus high-speed serial links for VXS connectivity.

(**Figure 2**). This switch card delivers high-speed switched serial interconnections on the standard VME backplane and targets embedded systems in the military, COTS (commercial-off-the-shelf), medical-imaging, and telecom markets. The IB4X-V41 has 18 payload connections, four interswitch connections, and two front-panel connectors that designers can convert to fiber through the use of a media converter. At the core of the switch is a single Mellanox Infiniscale III integrated-switch semiconductor providing 480-Gbps bandwidth. The air-cooled IB4X-V41-AC features two front-panel InfiniBand connectors, one 10BaseT/100BaseTx Ethernet port, and one RS-232 port. The fully managed switch card supports hot-swap functions. The IB4X-V41-AC VXS InfiniBand switch is available now for $7500.

Vmetro offers the Phoenix VPF1, a quad-signal-processing card for VME-based systems supporting the VITA-41/VXS standard. The VPF1 provides both dual PowerPC processors and dual Virtex-II Pro FPGAs, as well as two 4×, high-speed serial links for VITA 41 VXS standard fabric connectivity (**Figure 3**). "VXS provides a standard mechanism for high-performance, low-latency, board-to-board communications," says Andy Stevens, Vmetro's vice president. "It is perfect for those designers requiring efficient and scalable multiprocessing but who do not want to be locked in to proprietary systems." Vmetro also announced TransComm, a software library for VXS-based interprocessor communications to ease the programming burden with high-performance-multiprocessor applications. TransComm comprises routines that enable prioritized data movement and message passing between tasks; the tasks may reside on any processor, board, or set of boards connected through VXS-switched fabrics.

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For a related feature and a couple of related news and new-product items by Warren, see:

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MORE PINS, PLEASE

One of the major limitations of VME and even VXS is the number of signal pins interfacing to the backplane. Many system designers feel that the 335 signal pins of the P0, P1, and P2 connectors on a 6U VMEbus card are inadequate for modern, high-performance embedded-system projects. A pending VITA 46 update replaces the VMEbus connectors with a Tyco/FCI MultigigRT seven-row connector that provides high-speed serial fabric for all board-to-board communications (**Figure 4**). This modular connector comprises a series of interchangeable wafers for single-ended or differential pairs rated to 6.25 GHz and power. The wafers have their own ESD ground plane and contact layout to prevent accidental discharge during handling. The connector provides 48 single-ended signals and 192 differential pairs.

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10 bit	50 KSPS to 200 KSPS 200 KSPS to 500 KSPS 500 KSPS to 1 MSPS	**ADC101S021** **ADC101S051** **ADC101S101**	**ADC102S021** **ADC102S051** **ADC102S101**	**ADC104S021** **ADC104S051** **ADC104S101**
12 bit	50 KSPS to 200 KSPS 200 KSPS to 500 KSPS 500 KSPS to 1 MSPS	**ADC121S021** **ADC121S051** **ADC121S101**	**ADC122S021** **ADC122S051** **ADC122S101**	**ADC124S021** **ADC124S051** **ADC124S101**
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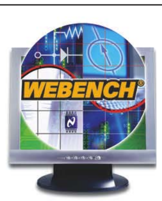

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The Sight & Sound of Information

Although dimensionally and electrically compatible with standard VMEbus modules, VITA 46 sacrifices backward compatibility to secure maximum performance. Savvy backplane designers have proposed hybrid VITA 46 configurations, even with the intentional incompatibilities, that allow each generation to coexist in the same chassis. Like the VXS standard, VITA 46 defines specific fabric configurations in subspecifications.

Although VITA 46 hardware has yet to appear, VMEbus manufacturers have developed product proposals to demonstrate the effectiveness of fabric systems. For example, the SVMX/DVMX-185 single-board computer from Curtiss-Wright Controls Embedded Computing is the first member of the company's VITA 46-based product line. This single-board computer will feature Freescale's 8641 PowerPC processor as well as integral high-bandwidth, low-latency ASI (Advanced Switching Interconnect) to exchange data with other single-board computers and I/O cards at fabric data rates. The SVMX/DVMX-185 also supports a bridging mechanism to support integration with RapidIO-based multicomputing clusters. The 185 will host two XMC (switched-mezzanine-card) modules, providing support for both PCI Express connectivity to the XMC and high-speed I/O from the XMC to the backplane. In addition, the SVMX/DVMX-185's ESD-protected connector system, with optional top and bottom covers, allows users to safely handle the device in flight-line environments in which standard ESD precautions are impractical.

The VMEbus standard has survived more than 20 years by balancing long-term system availability with strategic technology updates. Just as the standard seems doomed to obsolescence, clever designers have devised modifications that extend the bandwidth and retain compatibility with VMEbus hardware. Ray Alderman, VITA's executive director, said, "Unlike commodity-board markets, such as the telecommunications industry, VME appeals to markets that need intellectual-value-added applications. The aerospace, defense, manufacturing, and medical industries are great examples of those that need the values that VME provides."

Although the latest round of updates, VITA 41 and 46, allow VMEbus-embedded-system designers to move into the high-bandwidth realm of switched-fabric technology, new problems emerge. The failure of the market to adopt one fabric standard forces designers to make an educated guess and face interoperability issues with manufacturers that choose a different standard. The new VITA 46 connector arrangement will also create design headaches for designers that want to merge the new-generation hardware into older designs. EDN

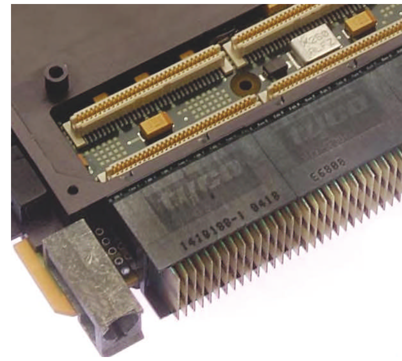

Figure 4 The pending VITA 46 update replaces the three VMEbus connectors and provides high-speed serial fabric for all board-to-board communications.

REFERENCE

1 Webb, Warren, "High-speed datapaths: Bypass bus bottlenecks," *EDN*, March 26, 1998, www.edn.com/archives/1998/032698/07cs.htm.

FOR MORE INFORMATION

Curtiss-Wright Controls Embedded Computing
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BY MICHAEL SANTARINI • SENIOR EDITOR

If three years ago you had asked EDA-software vendors about software piracy, they would have answered, "It's not a big problem." The addition of licensing software, such as FlexLM from Macrovision, to their tools acted as a good enough deterrent "to keep an honest man honest," in the words of one vendor. Now, in the age of WANs (wide-area networks), developers working on designs worldwide and 24/7, and ever-more-rampant EDA-software legal disputes, legal land mines are cropping up as fast as the pirates are finding new ways to profit. Accordingly, EDA-software vendors are taking software protection more seriously, and so should you.

Inadvertent piracy or use of stolen tools can put you at as much legal risk as people who bootleg and sell stolen software as their "business." So, EDA-industry organization EDAC (Electronic Design Automation Consortium) and its members are getting tough and pursuing the pirates. And, EDA vendor Silvaco, which two years ago won its misappropriation-of-trade-secrets case against Circuit Semantics, is now going after customers. It is attempting to recover the license fees for its software plus a percentage of revenue generated from products that those Circuit Semantics customers originally developed with Silvaco's stolen software. Among Silvaco's targets are AMD and Intel.

GETTING SERIOUS ABOUT PIRACY

Increasing complaints from its member companies and China's greater role in electronics prompted EDAC this year to establish a committee to gauge whether EDA piracy is real or an urban legend. It found that the problem is real, growing, and could wreak havoc on the $3.5 billion EDA market, according to Laurence Disenhof, a committee member and group director of export compliance and government relations at Cadence Design Systems. Disenhof says that the EDA industry is encountering more overt forms of piracy. "We are taking this seriously, and we think our customers will take it seriously, too," he says.

According to EDAC Piracy Committee member Jim Dou-

WHO ARE YOU BUYING YOUR EDA SOFTWARE

EDA-SOFTWARE VENDORS ARE TAKING SOFTWARE PROTECTION SERIOUSLY, AND YOU SHOULD, TOO. DON'T GET HOOKED ON PIRATED SOFTWARE.

FROM?

AT A GLANCE

- The Business Software Alliance estimates that pirates last year stole $31 billion worth of software.
- The most common cause of unintentional piracy in EDA comes from 24/7 worldwide use of a tool that one customer site originally licensed.
- EDA vendors offer 24/7 licenses, but they are more expensive than site-specific licenses.
- Users can be held liable for using software that vendors later prove is built on stolen code or trade secrets.
- Indemnification contracts are only as viable as the companies issuing them.

glas, Reshape's chief executive officer, cases of overt and inadvertent piracy are going on. "A lot of it is simply educating people and speaking with executives about the behavior of their organizations. They may be unaware of what constitutes inadvertent piracy, but, in other cases, they have employees that outright misuse and distribute software their company hasn't paid for," he said, as a member of a recent Design Automation Conference panel.

These problems are worse in countries outside North America and Europe and are especially bad for EDA in China and India. Altium fired its previous distributor in China after discovering that the distributor was selling Altium software on the side, and Altium's chairman claims his company has evidence that the Chinese government uses hundreds of pirated versions of Altium's Protel software for designing military equipment (see **sidebar** "China presents challenges for EDA"). Altium is pursuing this and related matters with the Australian government, which is currently negotiating a free-trade agreement with China.

WORLDWIDE PIRACY PROBLEM

EDAC and the BSA (Business Software Alliance), a nonprofit software-industry group dedicated to tracking and prosecuting software piracy, educating the public, and lobbying the government on the issue, have no statistics tracking the impact piracy has had on the EDA industry. But the BSA and industry analysts from research company IDC joined to conduct their first worldwide software-piracy study for the year 2003. And the most recent piracy study concludes that the software industry worldwide sold $59 billion worth of commercial software in 2004 but that $90 billion worth was installed, meaning $31 billion worth of software was pirated.

Although no study on EDA piracy exists, EDA vendors say convincing evidence does exist that EDA-software piracy is on the rise, especially as Asia opens up as a market for design tools. According to the 2004 study, Vietnam, Ukraine, and China top the list. In those three countries, 92, 91, and 90% of all software is stolen, respectively. In India, which has a growing reputation as a strong country in IC and design services, the figure is 74% (**Table 1**).

Laurie Atkinson, director of marketing at the BSA, says that the 2003 piracy study found that two-thirds of college students participating in the survey said that they have knowingly downloaded unlicensed software from peer-to-peer networks. "They know it is wrong, yet they do it anyway," she says. "And, presumably, they will be taking these attitudes into the workforce. When a company hires a new graduate, unless the company has an aggressive software-management policy in place, that new graduate may be illegally downloading software and putting that company into jeopardy."

Over the last year, you may have seen greater evidence and received a growing number of e-mail solicitations with URLs likely leading back to China or Russia, in which individuals claim to offer EDA tools at huge discounts. One such e-mail offers users unlimited access to any tool from Magma Design Automation, Mentor Graphics, Cadence Design Systems, or Synopsys for a low fee, and another claims to offer for $20,000 a workstation with every piece of EDA software from those vendors preloaded. The offer even includes maintenance. The BSA's director of enforcement, Jenny Blank, says that those offers are more likely to be Internet money scams than piracy operations. Still, no shortage of methods to pirate software exists.

TYPES OF SOFTWARE PIRACY

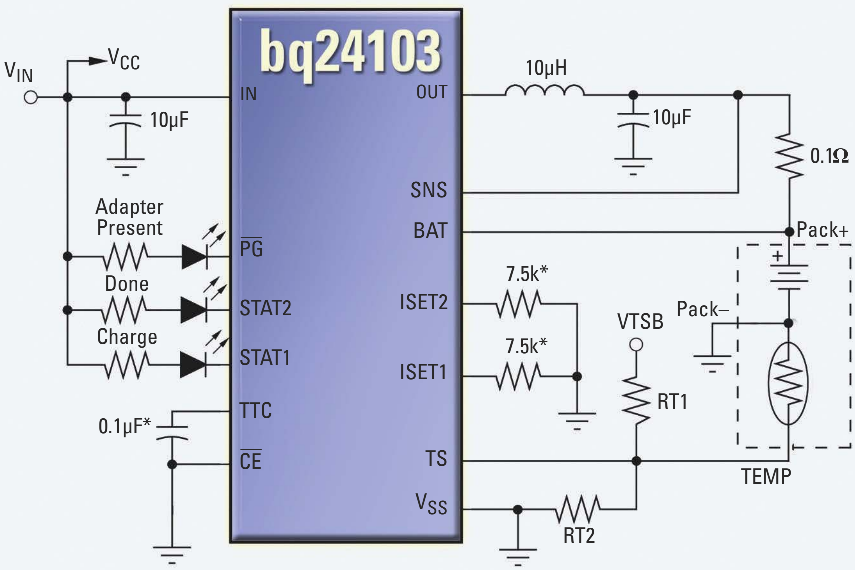
The BSA has identified five major classes of software piracy: end-user piracy, client-server overuse, Internet piracy, hard-disk loading, and software counterfeiting. End-user piracy occurs when a company employee reproduces copies of software without authorization. Client-server overuse occurs when too many employees access a piece of software over a network. Internet piracy takes place when pirate Web sites make software available for free download or in exchange for uploaded programs. It also occurs when Internet auction sites offer counterfeit, out-of-channel, infringing-

TABLE 1 SOFTWARE-PIRACY RATES

20 countries with the highest piracy rates	2004 (%)	2003 (%)	20 countries with the lowest piracy rates	2004 (%)	2003 (%)
Vietnam	92	92	United States	21	22
Ukraine	91	91	New Zealand	23	23
China	90	92	Austria	25	27
Zimbabwe	90	87	Sweden	26	27
Indonesia	87	88	United Kingdom	27	29
Russia	87	87	Denmark	27	26
Nigeria	84	84	Switzerland	28	31
Tunisia	84	82	Japan	28	29
Algeria	83	84	Finland	29	31
Kenya	83	80	Germany	29	30
Paraguay	83	83	Belgium	29	29
Pakistan	82	83	Netherlands	30	33
Bolivia	80	78	Norway	31	32
El Salvador	80	79	Australia	32	31
Nicaragua	80	79	Israel	33	35
Thailand	79	80	United Arab Emirates	34	34
Venezuela	79	72	Canada	36	35
Guatemala	78	77	South Africa	37	36
Dominican Republic	77	76	Ireland	38	41
Lebanon	75	74	Portugal	40	41

Courtesy Business Software Alliance

Integrated FET Switch-mode Charger



*I_{Charge} = 1.33A, $I_{Precharge}$ = 0.13A, Timer = 260 min

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bq24113	1- or 2- cell selectable	System-controlled	$2.20
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- Handheld devices
- Industrial equipment
- Medical equipment

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  - Reverse-blocking diode
  - Thermal shutdown
- Battery management features maximize capacity, cycle life and safety:
  - Accurate voltage and current regulation
  - Charge conditioning, status and termination
  - Battery detection
  - Safety timer
  - Temperature monitoring

▶ Packages

- 20-pin 3.5 x 4.5 mm^2 QFN
- Lead-free, RoHS-compatible

copyrighted software or when peer-to-peer networks enable unauthorized transfer of copyrighted programs. Hard-disk loading happens when companies load a piece of software onto multiple computer drives. And software counterfeiting occurs when users duplicate and sell exact copies of copyrighted material.

The two most common forms of piracy EDA vendors encounter are inadvertent piracy and intentional "overuser" perpetrators. You may be unaware that you are illegally using software. For example, EDA vendors offer companies a broad range of licensing options that can vary from sale to sale, so users need to be aware of the terms of their licensing agreements. "A majority of companies pirating software are actually honest companies, but, for whatever reason, software-asset management is just not at the top of their list of priorities," says Atkinson. She says that this situation typically occurs in the mid-sized- to small-business sector, which may lack full-time IT personnel to monitor these things.

According to Disenhof, the most worrisome form of piracy for the EDA industry is client-server overuse or, as many in the EDA industry call it, "underlicensing." "We are seeing one copy, one seat being purchased, then used 24 hours a day, seven days a week on a WAN," said Disenhof on a DAC panel. "This industry is using the Internet on a global basis today, and, whether they are doing it consciously or unconsciously, having software reside on a server that is accessed around the world may not be licensed legally. Engineers who are picking up the software in China, for example, during the graveyard shift in the United States may not have a legal right to use it. So, we are seeing a general trend of underlicensing across the board." Disenhof and others point out that most vendors offer terms that grant 24/7 usage of software worldwide, but it is typically much more expensive than a single-seat, perpetual license.

According to Rex Jackson, Synopsys' general counsel and acting chief financial officer, the other most common form of EDA piracy comes from the intentional overuser. A common profile of an inten-

CHINA PRESENTS CHALLENGES FOR EDA

EDA vendors see China as a potentially huge opportunity for market growth, but most agree that the Chinese government needs to be more diligent about creating and enforcing IP (intellectual-property)-protection laws to ease trade fears.

Altium's executive vice chairman, Kayvan Oboudiyat, says that Altium has been selling products into China for 12 years and has had an ongoing problem with the practice, as well as with piracy that Chinese consumers, businesses, and even the government perpetrate. "Protel tools are popular in China," says Oboudiyat. Many employers list Protel on their applications and list it as a qualification for new hires. But the number of qualified users far exceeds the number of licenses Altium has sold there. Part of that problem has been distribution in China. The company has for years sold its software through distributors in China but had to fire its first distributor in China after it found that the distributor was selling extra copies of Altium software on the side for its own profit.

"Although a majority of them were good, hardworking people, some of them were abusing their position, and, for every one license sold, they were selling a few more on the side," he says. The company has since taken steps to address that problem by establishing an office in Shanghai and by hiring new resellers. "The only way we can effectively address this issue is by working with resellers and customers and educating them that there is more to EDA products than just the CDs. You can go to any software shop in Shanghai, Beijing, or Shenzen and buy an illegal version of Protel over the counter. We need to develop a relationship and an emphasis on the value of training."

The Chinese government has also been ineffective in policing the problem, and Oboudiyat says that, in Altium's case, it has even been a culprit in some instances. "There is a lot of goodwill on the part of the Chinese government, but they need to make some radical changes to become effective," says Oboudiyat. "We know and have solid evidence that some of the largest government-owned military-R&D organizations in China use not just tens but hundreds of illegal licenses. We need to develop relationships with the government and come up with a long-term, sustainable solution."

Part of the problem may be cultural, vendors and BSA members say. "I don't know that the Chinese people who do what we think is stealing software actually think they are stealing software," says Rex Jackson, Synopsys' general counsel and acting chief financial officer. "I don't know that they look at it that way."

To change this situation, all agree education about international law is paramount, but money will ultimately be the factor that makes things change in China. Others point out that, as Chinese companies start to acquire international companies, adoption of international IP laws will also speed up. Most vendors believe it will just take time. Most point to Taiwan as a prime example, saying that piracy was once rampant, but the problem has decreased as the country plays a larger role in the international business community. "I think it is going to change, perhaps not as fast as we would like, as the Chinese develop their own IP," says Jackson.

Some large Chinese companies have approached Altium, admitting that they inadvertently own pirated copies of Altium's software and want a formal, legitimate relationship with the company. "In these cases, we've worked with customers to resolve issues and form long-term relationships," says Oboudiyat. "Over the next five to 10 years, this approach will become a common way to deal with the issue of piracy."


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tional overuser is a customer who acquires just one perpetual license of a flow and then almost immediately drops the maintenance agreement. "We work with our salespeople to identify that profile because it is remarkable how good that match is," says Jackson. "Once you have identified customers that came in once and then disappeared off the radar screen, you have to ask yourself: Do they still exist, where are they, and how large do you think their design team is?"

Jackson says that all Synopsys contracts give the company the right to audit users to ensure they are not misusing licenses, and Synopsys exercises this right, especially when customers fit the intentional-overuser profile. Synopsys and most EDA companies tend not to pursue every small infringement, simply because doing so is not cost-effective. Synopsys, like many EDA companies, has joined the BSA and is banking on the fact that education on all levels is the key to reducing all forms of piracy over time.

The BSA helps to educate consumers, businesses, and government officials worldwide about software piracy. Failing that, the BSA also has legal muscle, a Public Action Committee, to push for domestic and international legislation regarding software piracy. It also runs piracy hot lines in most countries.

LEGAL CONSEQUENCES

The BSA's Blank says that the BSA helps its member companies bring civil suits against offenders, works with criminal-law-enforcement authorities, and operates a high-volume notice-and-takedown program. Both inadvertent and overt software pirates can face criminal charges ranging from fines to jail terms. The FBI doesn't get involved until the amount of software pirated exceeds $100,000, a lofty amount for business-software pirating but the price of only one or two tools for pirated IC EDA tools, whose prices average approximately $40,000 per seat.

Vendors in the United States can seek one of two civil-court remedies if they catch a company or an individual stealing. The first is a $150,000 fine plus the cost of the software. According to Blank, vendors take this tack in 99% of piracy cases in the United States. The second remedy is an open-ended civil damage for recovering not only the loss of license, but also a percentage of the revenue pirates generate using end products they developed with the stolen software. Users can also be in legal jeopardy if they use one vendor's product that is later found to infringe another company's patent, copyright, or trade secret. "Under the federal Uniform Trade Secret act, customers have full liability if they are using software that infringes a patent or if they purchase software that is stolen," says Chris Scott Graham, IP (intellectual-property) attorney with Dechert LLP, a law firm that currently represents both Silvaco and Synopsys on their respective IP litigations. California district attorneys can prosecute engineers under Criminal Trade Secret Statute 499C for using a product that violates a trade secret or under the California Penal Code Section 496, which essentially states that receiving any stolen property is a crime.

SILVACO SEEKS LEGAL REMEDY AS SYNOPSYS WATCHES

Users have so far largely ignored the legal wrangling of EDA vendors and continued to use software even if a preponderance of court evidence indicates that the software is tainted. They made this decision largely because they believed EDA vendors had no recourse. They assumed that vendors would not risk losing current or potential customers. Also, they had received indemnification from the vendor from which they had licensed the software.

Silvaco is attempting to debunk this idea and is pursuing former Circuit Semantics customers. In 2003, Silvaco won its misappropriation-of-trade-secrets suit against EDA start-up Circuit Semantics. In that suit, the court ordered Circuit Semantics to relinquish ownership of its misappropriated source code and other products to Silvaco. According to Chris Scott Graham, Silvaco's attorney with law firm Dechert LLP, Silvaco is now pursuing its right to recover the cost of the stolen license from those customers as well as a percentage of revenue from any products developed with the stolen software.

For a relatively small company such as Silvaco, the move appears to be a gamble. Silvaco risks burning the bridge that links it to some of the EDA industry's biggest customers. Silvaco officials won't comment, but the company's president and owner, Ivan Pesic, comments extensively at www.deepchip.com, an EDA-industry-observing Web site. Vendors have threatened to pursue customers but usually have not done so. Cadence, for example, didn't pursue Avanti customers after Avanti officials pleaded no contest in criminal court to stealing Cadence code. And Synopsys, which appeared well on its way to winning a trade-secret suit against Nassda before acquiring that company last year, didn't pursue customers because it ended up inheriting Nassda contracts.

But Synopsys' Jackson says that the company hasn't ruled out going after Magma customers, especially those that have continued to license software from Magma even after Synopsys' legal team presented what appears to be damning evidence in the form of Magma cofounder Lukas Van Ginneken's admitting that he used technology developed at Synopsys to design Magma's products. "Our focus is on winning the Magma case first," says Jackson. "We'll see where it goes from there. I am surprised that, in the EDA business, customers figure it won't be their problem and that someone will work it out so that they don't have to worry about it. I don't understand that perspective. I would never say that I'm going to sue everybody that uses Magma tools if we win the Magma case. In the interim, though, given how clear the admissions have been in the Magma case, it surprises me that people would make new commitments to that technology."

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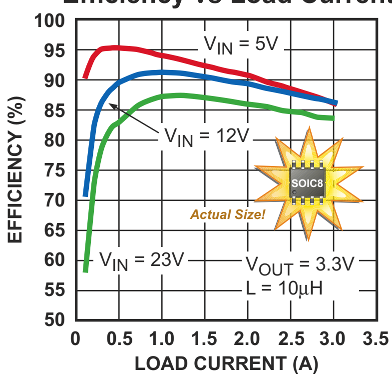

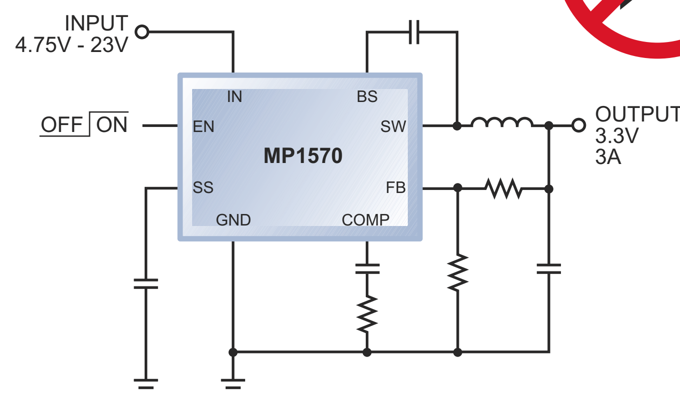

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MP2106	800kHz	2.6 - 13.5	1.5	QFN10 (3x3)
MP2305	340kHz	4.75 - 23	2.0	SOIC8
MP1570	340kHz	4.75 - 23	3.0	SOIC8
Featured Non-Synchronous Bucks				
MP2361	1.4MHz	4.75 - 23	1.5	QFN10 (3x3)
MP2364*	1.4MHz	4.75 - 23	2x 1.5	TSSOP20
MP2354	380kHz	4.75 - 23	2	SOIC8
MP1593	385kHz	4.75 - 28	3	SOIC8

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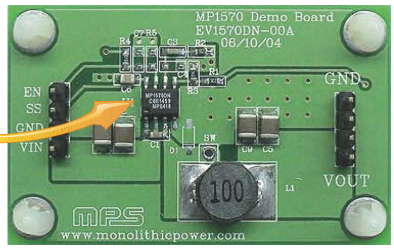

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Although EDA vendors commonly sue each other in civil court in patent or trade-secret disputes, EDA vendors have traditionally shied away from suing customers that use infringing software. Silvaco is bucking that trend, and, pending the conclusion of its suit against Magma, Synopsys hasn't ruled out pursuing Magma customers, either (see **sidebar** "Silvaco seeks legal remedy as Synopsys watches").

HOW TO PREVENT PIRACY

Most EDA tools include security technology such as Macrovision's FlexLM, which essentially functions as a key that allows access to the software for the term of the license. However, the use model for EDA software has been changing and has become more complex. Traditionally, vendors have sold licenses on a per-CPU or per-seat basis, but Suresh Balasubramanian, director of licensing products at Macrovision, says that licensing arrangements are getting more complex because user demands and even the definition of "CPU" are changing. "In the semiconductor industry, we are seeing a trend toward deploying software on mass-computing, where people want to do bigger simulation faster and deploy these jobs on thousands of CPUs," he says. "When you look at new technology trends, where the whole dynamic of computing changes—where you have dual-core CPUs or multithreaded CPUs—publishers are often at a loss as to how to license their software." Macrovision is working with other vendors to do intelligent scheduling to monitor simulation-farm usage. The company is also looking at developing programs to prevent pirates from overtly hacking EDA software (see **sidebar** "How pirates hack EDA software"). "Just as people are determined to break software, one of the things we've put in our software is for crippling pirated software," Balasubramanian says. "So, for example, if someone pirates an EDA tool, their verification won't complete, or their timing will be off, so you frustrate the hell out of them and ensure that they are not productive."

Of course, EDA software doesn't have the greatest reputation for being bug-free. Half-jokingly, vendors agree that EDA lends itself less well to piracy because its software tends to be complex and bug-prone, requiring upgrades and maintenance. Ironically, some vendors say they discovered that they had a piracy problem when an increasing number of non-customers inquired about software patches or sent inquiries to customer support or even formed user groups in countries not allowed to own EDA software. EDA vendors pass the cost of adding greater licensing and security features to their products onto their customers.

HOW TO PROTECT YOURSELF

Due diligence is the key, experts say, to protecting yourself or the company you work for from implication in a software-theft-related lawsuit. Designers and managers need to be aware of the terms of their software-license agreements, and, for example, not access any software that has a geography- or site-specific license. Companies also need to police their employees to ensure that they are not bootlegging corporate products for their own personal use or profit. Experts say that your company, as well as the individual employee unknowingly perpetrating the crime, can incur huge fines. According to the BSA, the most common way that companies discover piracy is after a disgruntled employee reports it. If your company is using software that is stolen and such an employee reports it, the piracy can damage your company, division, or group to the point that you may find yourself out of a job.

If you are licensing software from a vendor that is later sued or is currently being sued by another vendor for patent or copyright infringement or misappropriation of trade secrets, that other party can also sue you if doing so ultimately wins the legal dispute. Because of this risk, experts say that customers have every right to demand to see all pertinent evidence in the case to assess whether the vendor can win the case or is healthy enough to honor indemnification if it loses the suit.

"Indemnification is a contractual agreement that says, 'If I'm found to have stolen someone's product, I will replace what I sold you with a noninfringing copy, or I will refund your money or defend you from a third party claiming you have done something wrong,'" says Graham. "In most cases, indemnifications are not worth the paper they are written on." Graham notes that insurance companies do not back indemnification contracts, and, therefore, any indemnification contract is only as strong as the size, health, and cash balance of the company offering it. **EDN**

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HOW PIRATES HACK EDA SOFTWARE

Suresh Balasubramanian, director of licensing products at Macrovision, says that Macrovision-licensing software developers are in a cat-and-mouse game with hackers. Balasubramanian says that people have illegally hacked into EDA software in three ways. The first way is by configuring multiple workstations or computers to appear to the license as just one computer. Vendors roughly three years ago defeated this approach. Once defeated, hackers then started illegally generating license keys to perpetually access software. Advanced encryption technology from Cirticom a couple of years ago defeated that approach. Hackers now have to enter the binary code and hack the licensing code. Balasubramanian says that a version of FlexLM, slated for release this year, will allow users to distribute that code throughout their program and tie it closely to functions, so if someone hacks a code, the tool will run but give inaccurate results.

You can reach
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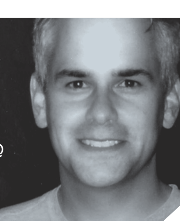

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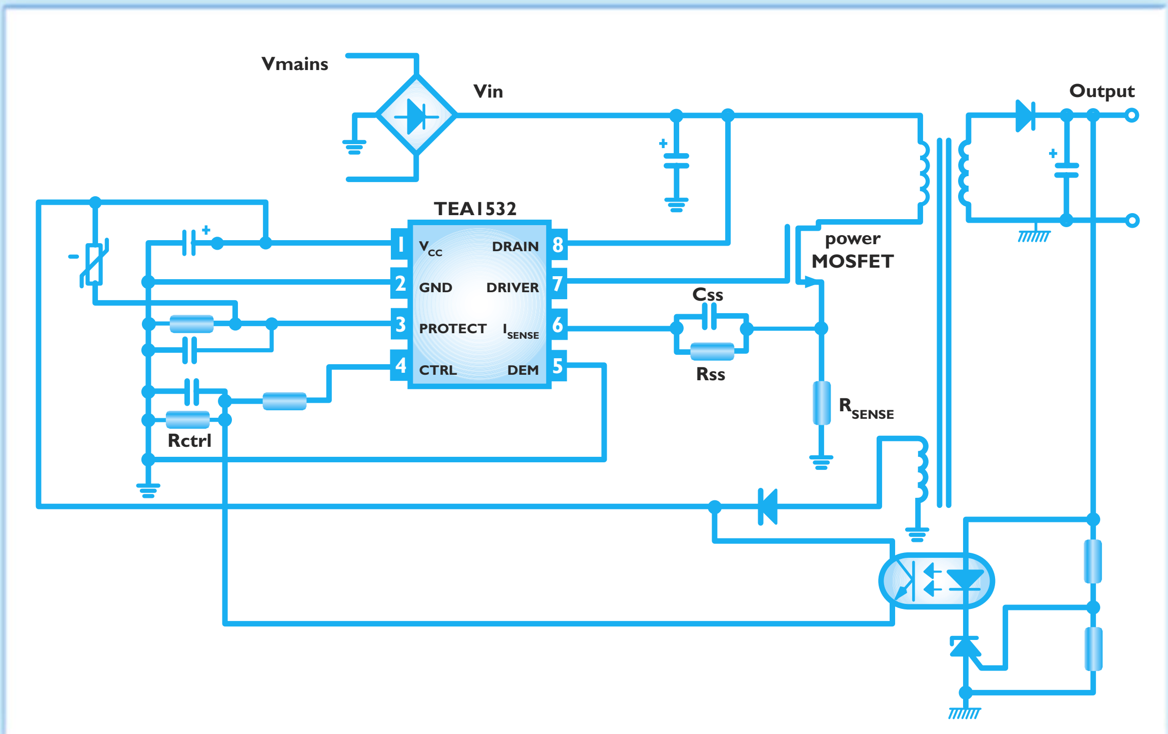

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NATIONAL INSTRUMENTS

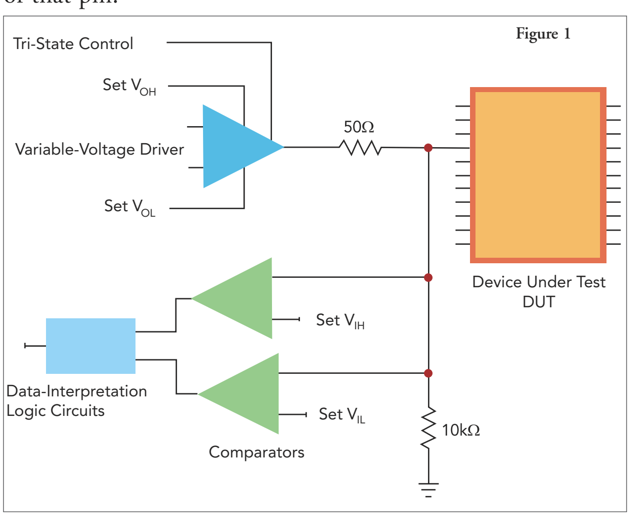
THE DATA DETECTIVE

Digital Data Hits Highs and Lows

When testing digital circuits, engineers stimulate inputs and monitor outputs to determine whether or not devices or circuits work properly. Thankfully, software can take a design and create a pattern, or vector, of 1's and 0's that test equipment can automatically apply to digital inputs. A mismatch between a device's actual and expected output indicates a fault.

Many manufacturing faults of digital components fall into one of the following categories: open circuits, short circuits, or stuck-at faults. The latter group divides into stuck-at-1 or stuck-at-0 faults, which means an output remains "stuck" at a logic-1 or a logic-0 level.

Most equipment used to test digital circuits includes both a voltage driver and comparators for each channel, as shown in the figure below. These pin electronics let test engineers stimulate a device's digital input as well as monitor the state of that pin.



The circuit above, similar to those found on the National Instruments NI-655x waveform-generator/analyzer cards, includes independent stimulation and measurement electronics that operate simultaneously. Each pin requires its own driver and comparator circuit.

The variable-voltage driver shown in the figure will generate a high output voltage (V_{OH}) or a low output voltage (V_{OL}) to produce a logic-1 or a logic-0 at the input of a device under test (DUT). The driver circuit also can present a high impedance to the DUT, in effect disconnecting the driver portion of the pin electronics from the circuit. Programmable V_{OH} and V_{OL} levels let this circuit drive ICs in many logic families. The 50-Ω series resistance at the driver's output enhances signal integrity.

Measurements at the driver's pin involve two comparators, one that compares the DUT's output voltage to a low acquisition voltage (V_{IL}) and another that compares the DUT's output to a high acquisition voltage (V_{IH}). (Software will preset these voltages, depending on the tests an instrument requires.) Logic circuits connected to the comparators in the pin electronics determine whether the DUT produced a valid logic 0 or logic 1. In the event of a fault, this logic also can determine if the DUT has produced an invalid output between the preset V_{IL} and V_{IH} levels. The comparator circuit provides a known input impedance—a 10-kΩ resistor that connects to ground. Note the comparator circuits operate independent of the voltage driver, so the digital test equipment can simultaneously stimulate a pin as well and measure the voltage on it.

To test a device, digital test equipment can apply a "marching 1" pattern—1000.., 0100.., 0010.., and so on—to a DUT's pins. The tester monitors the DUT's pins to ensure the detected pattern matches the output pattern produced by the driver electronics. If a marching-1 pattern produces logic 1's at two or more pins, a short may exist between those pins. Likewise, if the driver applies voltage and not enough current flows—as detected by the comparators—the circuit may have an open. (Tests also may use a marching-0 pattern; 0111.., 1011.., 1101.., and so on.)

Stuck-at faults usually appear when a conductor shorts to a power-supply (Vcc) or ground connection. During a marching-1 or a marching-0 test, for example, a stuck-at pin will appear as an extra 0 or 1 in the pattern. Generally, no amount of stimulation will change the state of a stuck-at pin.

Don't worry about constructing pin electronics—companies offer them for buses such as PXI and VXI, and they come as part of some automatic test equipment (ATE). Companies also offer test-development software.

The Chips are Down

Chris received the first batch of digital ICs he designed to operate at a custom voltage. Much to his dismay, initial tests show no chips work. Chris plans to use a digital I/O board to determine whether the problems exist in his design or in the silicon.

To help Chris test the chips and discover the problem, go to

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Go to http://rbi.ims.ca/4395-502 to solve the challenge!

TECH TRENDS DAN STRASSBERG • CONTRIBUTING TECHNICAL EDITOR

VNAs and TDRs: taking the measure of the new millennium

PASSIVE-COMPONENT TESTING IN WHAT WILL SOON BE THE 10-GHz ERA REQUIRES SPECIALIZED TOOLS. FORTUNATELY, USING THOSE TOOLS NO LONGER REQUIRES EXPERTISE IN FIELDS IN WHICH FEW DIGITAL DESIGNERS ARE PROFICIENT.

The ZVT8 VNA measures characteristics of multiport and differential devices over a 300-kHz to 8-GHz range. The system provides eight ports and offers a dynamic range of 120 dB and a maximum output power of 13 dBm at all ports. A reflectometer at each port even allows simultaneous measurements on several multiport devices (courtesy Rohde and Schwarz).

Despite passive components' rather unglamorous image, the only way to do justice in print to the subject of testing the devices would be to write a sizable book or a long series of articles. With the format limited—for now, at least—to just one article, a more appropriate approach is to pick a small subset of the enormous universe of passive devices and a few of the many classes of instruments that EEs use to test components of the selected types.

So it is, then, that this article focuses on VNAs (vector-network analyzers) and related instruments, such as TDRs (time-domain reflectometers). VNAs comprise a poorly understood class of generally expensive instruments—prices start in the neighborhood of $30,000—that, until recently, have been the province mainly of microwave engineers. The mathematical and analytical tools, S-parameters (scattering parameters), and Smith charts (see **sidebar** "S is for Smith chart and S-parameters"), which microwave engineers use with VNAs, often bewilder and sometimes strike terror in the hearts of EEs who lack high-frequency-design backgrounds.

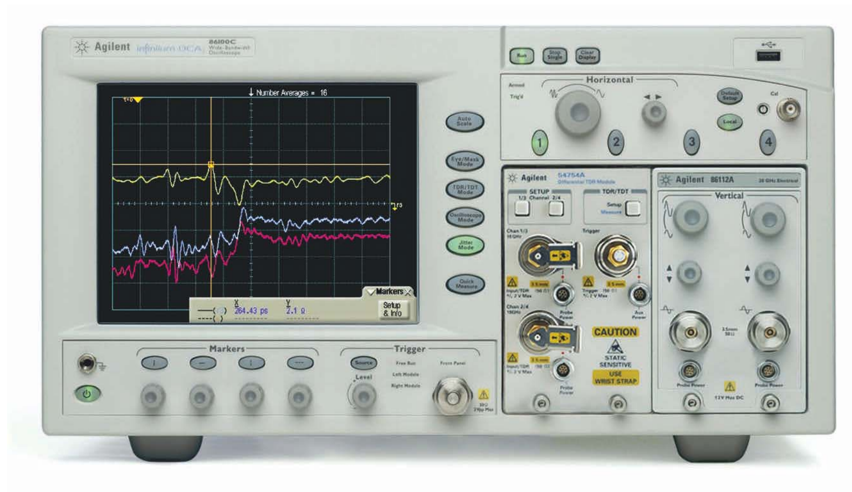
A key reason for focusing on VNAs is the explosion of interest in wireless communication, much of which takes place at 2.4 GHz, 5 GHz, and even higher frequencies. At these frequencies, lumped-circuit models simply don't adequately describe component and network behavior, making distributed-circuit analysis mandatory. Most work done by and with VNAs relates to linear circuits—those in which superposition holds. But some companies make LSNAs (large-signal network analyzers), which are usable with networks that contain nonlinear elements and with active circuits that exhibit nonlinear behavior when driven by large signals.

Despite a reputation for inscrutable user interfaces, VNAs are not especially difficult to grasp, as long as you limit the discussion to basic concepts. Moreover, with the widespread adoption of DSP,

AT A GLANCE

- Characterizing passive components for use at multigigahertz frequencies is exacting work that requires precision instruments and fixtures and consummate care.
- VNAs (vector-network analyzers) hold the key to the necessary measurements but until recently were known as difficult to use by engineers without microwave expertise.
- Newer VNAs incorporate intelligence to simplify their user interfaces, DSP to enable time-domain presentation of frequency-domain-measurement results, and additional ports to facilitate increasingly common measurements on differential structures.
- High-performance TDRs (time-domain reflectometers), though lacking VNAs' dynamic range, can offer a somewhat lower cost alternative to VNAs in some applications.
- Both TDRs and VNAs require high-quality device-under-test fixturing and mathematical de-embedding of fixture and cable effects from measurement results. VNAs also require calibration. Automation now drastically simplifies de-embedding and calibration.

most VNAs can present in the time domain the results of measurements they make in the frequency domain. Time-domain capabilities, automation of many functions, and burgeoning use of built-in intelligence to create simpler interfaces have arrived in VNAs just when users really need them. Friendliness to users who aren't microwave engineers is rapidly becoming essential because, as the clock rates in ICs and on pc boards ratchet upward, increasing numbers of digital-hardware designers need to characterize components at frequencies at which only VNAs can make the necessary measurements with the required accuracy. Most of these designers feel much more comfortable working in the time domain than in the frequency domain.



You can now equip the Windows-based 86100C digital-communications analyzer–at heart, an ultrawideband sequential-sampling scope–with software that enables the instrument to present as S-parameters the results of measurements made with a TDR plug-in (courtesy Agilent Technologies).

However, for microwave engineers who are at home with S-parameters, Agilent, which manufactures both VNAs and TDRs, now offers for its 86100C DCA (digital-communications analyzer) software that extracts S-parameters from TDR data. Thus, users can take their pick—measure in either the time or the frequency domain—and present the data in its native domain or in the complementary one. The slogan, "have it your way," thus applies to products a lot more complex than hamburgers.

JUST A MATTER OF TIME

Agilent's new software underscores the fact that the frequency and time domains merely represent different ways of looking at the same phenomena. By applying a swept-frequency sine-wave stimulus to a DUT (device under test) and making measurements with detectors tuned to the stimulus frequency, a VNA accomplishes essentially what a TDR does when it applies a repetitive voltage step to the DUT and examines the reflected signal at the input port. The TDR performs its examination in the time domain, however, using high-speed sequential-equivalent-time-sampling-oscilloscope technology. In the TDT (time-domain-transmission mode), a TDR instrument can also examine the transmitted signal at another port, just as a VNA can measure transfer characteristics among a multiport device's several ports.

The VNA's advantage over the TDR is that the dynamic range of its measurements is inherently greater—by as much as 80 dB. And though VNAs often cost significantly more than TDRs, they don't cost 80 dB more; that is, they don't cost 10,000 times or even 100 times as much. Also, modern VNAs' frequency sweeps can be quick. Except when measuring at their highest dynamic ranges, these instruments often measure approximately as fast as do TDRs. A high-performance TDR is built around a high-performance sequential-sampling scope in which is mounted a TDR plug-in that contains a repetitive-step (pulse) generator as well as a sampling circuit. You would probably need the scope even if it didn't do TDR. If adding appropriate software to the scope enables it to make S-parameter measurements that meet your requirements, you may well be able to do without the VNA and thus save its considerable cost.

TDRs also claim an advantage over VNAs in simplicity of—and even absence of the need for—calibration. However, manufacturers of probers for use with VNAs and systems that use VNAs say that automatic VNA calibration is much faster—minutes versus hours—than the manual calibration that VNAs used to re-

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quire. Further, they say, automatic calibration provides more accurate and repeatable results (5% uncertainty versus 20% or more) at frequencies of 40 GHz and more (**Reference 1**).

With both TDRs and VNAs you must extract (de-embed) from your measurements the effects of the fixturing and cables that connect the DUT to the instrument. De-embedding requires you to measure and mathematically characterize the effects of these measurement-system components and then mathematically remove the effects from the measured data. The resulting data should then represent the characteristics of the DUT alone. The computations are usually far from trivial, but modern, high-performance instruments automate de-embedding so that you can often avoid becoming intimately involved with it, although you probably will have to choose a calibration strategy (**Reference 1**).

INHERENTLY GREATER RANGE

There are two main reasons that a VNA's dynamic range is usually greater than a TDR's. The VNA uses a swept-tuned narrowband detector whose internal noise is inherently much lower than

S IS FOR SMITH CHART AND S-PARAMETERS

The (circular) Smith chart (Figure A) is a transformation of the complex impedance or admittance plane into a polar plot of the complex reflection coefficient, Γ, which is often described in terms of magnitude, ρ, and phase, ϕ. On impedance charts, it is customary to normalize to 1Ω the characteristic impedance, Z_0 (usually 50 or 75Ω), which appears at the center of the chart and is purely resistive for lossless transmission lines. Although the quantities plotted on a Smith chart are frequency-dependent, frequency does not appear explicitly in the coordinates. Instead, it appears at points along the curves plotted on the chart.

A short circuit is at the left end of the horizontal axis that divides inductive impedances (R+jx), which appear in the upper half of the chart, from capacitive impedances (R−jx), which appear in the lower half. An open circuit lies at the right end of the horizontal axis. Pure reactances lie along the outer, circular edge of the chart, where Γ=1. Any arbitrary point on an impedance Smith chart that is not in the center or along the outer edge is a series combination of a finite resistance and a finite reactance, either inductive or capacitive. For an admittance Smith chart, any arbitrary point is a parallel combination of a finite resistance and a finite reactance, either inductive or capacitive (which is the same as a series combination of conductance and susceptance).

Smith charts are popular with microwave engineers, who, with a little practice, can use the charts to quickly and intuitively solve many problems in passive and active microwave-network design. VNAs can present reflection data on their screens in Smith-chart form and, when connected to an appropriate printer or plotter, can also produce printed Smith charts. Analog Instruments, the company founded by the late Bell Laboratories engineer, Philip H Smith, who devised the chart approximately 70 years ago, still exists. A few years ago, the company, which copyrighted the name "Smith chart," claimed to still be shipping nearly a million pounds per year of blank Smith-chart forms to corporate customers.

S-parameters (scattering parameters) are derived from direct measurements of reflection and transmission coefficients. You can also derive them by taking the inverse FFT of time-domain parameters, such as reflection coefficient, rho-p, which you can measure directly with a TDR (time-domain reflectometer). Reference A contains tables that convert S-parameters to and from conductance parameters (y), resistance parameters (z), and a mixture of conductance and resistance parameters (h).

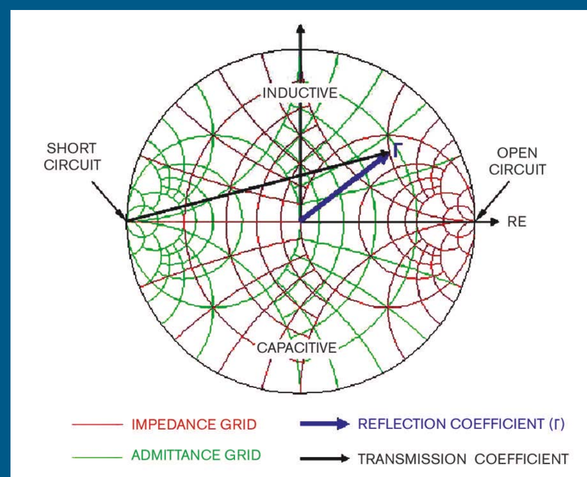

Figure A The Smith chart is a transformation of the complex impedance or admittance plane into a polar plot of the complex reflection coefficient (courtesy Microwave101.com).

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B Agilent–EESof, "Basics of S-parameters, Part 1," http://eesof.tm.agilent.com/docs/iccap2002/MDLGBOOK/1MEASUREMENTS/3VNA/3SPAR/1SparBasics_1.pdf

(For Part 2 of Reference B, replace _1.pdf at the end of the above URL with _2.pdf .)

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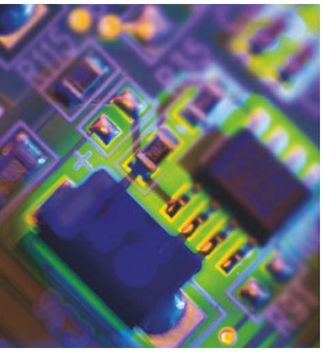

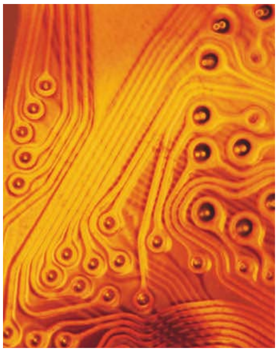

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that of the wideband detector that the TDR must use. Also, the amplitude of the VNA's sinusoidal stimulus signal remains relatively constant as its frequency varies. In contrast, the amplitudes of the various frequency components of a TDR's output step necessarily decrease in proportion to their harmonic number. Therefore, the high-frequency content of the TDR step is much lower than that of the VNA's swept-frequency stimulus. VNAs also provide greater high-frequency accuracy than do TDRs because of the difficulty that TDRs encounter in generating sufficiently fast voltage steps and delivering them unimpaired to the DUT.

The highest frequency VNAs measure directly to approximately 110 GHz and to approximately 320 GHz with external frequency-translation (downconversion) hardware. The widest-bandwidth sampling oscilloscopes, such as those in high-performance TDRs, have bandwidths that approach and, in one case, equal 100 GHz. But a wideband detector isn't all you need to build a 100-GHz TDR. The instrument would also need to stimulate a DUT with a voltage step whose 10-to-90% rise time was less than approximately 4.5 psec. The generator that currently produces the fastest rising differential-TDR pulse supplies pulses with a rise time of approximately 9 psec. Moreover, delivering these pulses to the DUT without degrading the rise time and introducing other signal anomalies requires consummate care. Because a VNA sends sine waves rather than voltage steps to the DUT, connecting it to the DUT might seem to be less challenging, but at the frequencies involved, fixturing the DUT for the VNA requires as close attention as does fixturing it for the TDR.

A frequently asked question is how a VNA differs from a swept-frequency SA (spectrum analyzer) coupled with a frequency-tracking signal generator (see **sidebar** "Comparing VNAs with SAs"). A key difference is that an SA—without the generator—characterizes signals, and a VNA characterizes networks or components. However, whereas a VNA measures the phase as well as the magnitude of the signals it receives, relatively few SAs measure phase. Without the phase information, the instrument can't correctly reconstruct nonsinusoidal waveforms by combining their frequency components. Thus, to make the transition from the frequency domain to the time domain, the phase-versus-frequency information is essential.

As digital-system designers well know, differential signaling is central to increasing digital-system clock rates. The technique relaxes requirements for low ground-plane inductance, reduces ground

COMPARING VNAs WITH SAs

By David Ballo, Agilent Technologies

An SA (spectrum analyzer) and a TG (tracking generator) form a stimulus/response system. An SA/TG combination can measure transmission, but, to measure reflection, the SA/TG combination also needs a device that can separate the reflected signal from the incident signal. Either a directional bridge or a directional coupler can perform this function. Compared with an SA/TG combination, the VNA (vector-network analyzer) provides three clear advantages:

Convenience: On a two-port device, the SA/TG can measure only one thing at a time (for example, forward transmission or reverse reflection), whereas a two-port VNA can measure all four S-parameters (scattering parameters) with the same setup (forward transmission and reflection and reverse transmission and reflection). A four-port VNA offers even more convenience for measuring balanced devices than does the SA/TG pair. The VNA can measure 16 S-parameters at once, as opposed to one at a time with the SA/TG combination.

Phase: Most SAs have only one receiver and can measure only a signal's amplitude. Testing components' phase response requires measuring the phase difference between the test signal and the incident signal, which requires at least two receivers. (VNAs typically have three or four receivers to measure both forward and reverse responses.) Some SAs, such as VSAs (vector-signal analyzers), can measure phase, but they analyze modulation phase relative to a carrier. Although some VSAs have two receivers to measure ratioed phase, the modulation bandwidth of signal generators and VSAs is usually insufficient to cover the frequency range required for testing the in-band and out-of-band responses of passive components.

Accuracy: VNAs use sophisticated mathematics to remove the undesired effects of the test system, such as cable loss and mismatch versus frequency. This level of error correction requires magnitude and phase information. To correct system errors, an SA can do only simple normalization, which results in much less accurate measurements. For example, in high-frequency measurements, normalization cannot remove the error ripple caused by the mismatch between the test-system cables and the input or output match of the device under test.

AUTHOR'S BIOGRAPHY

David Ballo is product-marketing engineer with Agilent Technologies (Santa Rosa, CA), where he is responsible for the PNA series of VNAs. He has more than 24 years of RF- and microwave-measurement experience. He holds a bachelor's degree in electrical engineering from the University of Washington (Seattle).

bounce, and, compared with single-ended signaling, allows smaller signal swings. As it turns out, VNA technology was fairly well-prepared for differential signaling long before the technique became popular. Two single-ended VNA ports can interface with one differential DUT port, and nearly all VNAs have at least two single-ended ports. Although there are techniques that you can sometimes use to interface one single-ended VNA port to a differential DUT port, a VNA with only two single-ended ports is usually unsatisfactory for characterizing transmission properties through networks with differential inputs and outputs. For that task, you are likely to need a VNA with four single-ended ports, configured as two differential ports. Moreover, complex networks that require still more VNA ports are becoming increasingly common. In response, VNAs with more ports are also becoming more common. For example, Rohde and Schwarz recently introduced an eight-port instrument. Nevertheless, with appropriate software, two-port VNAs can make many measurements that EEs need to perform on differential networks, and one vendor reports that it continues to ship many more two-port VNAs than units having larger numbers of ports. The reason, of course, is that instruments with fewer ports cost less. EDN

MORE AT EDN.COM

For more on the Smith charts mentioned in one of this article's sidebars, see www.edn.com/article/CA56700.

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FOR MORE INFORMATION

Suppliers of vector-network analyzers:

Agilent Technologies
www.agilent.com

Anritsu
www.global.anritsu.com

Maury Microwave
www.maurymw.com

NMDG
www.nmdg.be/start.html

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Suppliers of high-performance time-domain reflectometers:

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Suppliers of probes, probe stations, and VNA-calibration accessories:

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Suppliers of other component-test instruments and systems:

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Suppliers of consulting services and software related to VNAs and TDRs:

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LINEAR TECHNOLOGY DESIGN NOTES

Industry's First 4-Switch Buck-Boost Controller Achieves Highest Efficiency Using a Single Inductor – Design Note 369

Wilson Zhou and Theo Phillips

Introduction

One of the most common DC/DC converter problems is generating a regulated voltage that falls somewhere in the middle of a wide range of input voltages. When the input voltage can be above, below or equal to the output voltage, the converter must perform step-down and step-up functions. Unlike solutions requiring bulky transformers, the LTC®3780 meets these requirements in the most compact and efficient manner, using just one off-the-shelf inductor and a single current sense resistor.

The LTC3780 uses a constant frequency current mode architecture which allows seamless transitions between buck, boost and buck/boost modes with a wide 4V to 30V (36V maximum) input and output range. Burst Mode® operation and skip cycle mode provide high efficiency operation at light loads, while forced continuous mode and discontinuous mode reduce output voltage ripple by operating at a constant frequency. A soft-start feature reduces output overshoot and inrush currents during start-up. Overvoltage protection, current foldback and on-time limitation provide protection for fault conditions, including short circuit, overvoltage and inductor current runaway. The LTC3780 is available in low profile 24-pin TSSOP and 32-lead 5mm × 5mm QFN packages.

High Efficiency 4-Switch Buck-Boost Converter

Figure 1 shows a simplified LTC3780 4-switch buck-boost converter. When V_{IN} exceeds V_{OUT}, the LTC3780 operates in buck mode. With switch D on and switch C off, switches A and B turn on and turn off alternately, as they would in a typical synchronous buck regulator. Conversely, when V_{IN} is lower than V_{OUT}, the LTC3780 operates in boost mode. With switch A on and synchronous switch B off, switch C and synchronous switch D turn on and turn off alternately, behaving as a typical synchronous boost regulator.

When V_{IN} is close to V_{OUT}, the controller is in buck-boost mode. Switches A and D are on for most of each period. Brief connections between V_{IN} and ground, and V_{OUT} and ground, are made through the inductor and switches B-D and A-C to regulate the output voltage. In buck-boost mode, inductor peak-to-peak current is much lower than that of SEPIC converters and traditional buck/boost converters. Figure 2 shows the inductor current and switch node waveforms.

Low inductor ripple current and the use of synchronous rectifiers allow the LTC3780 to achieve very high

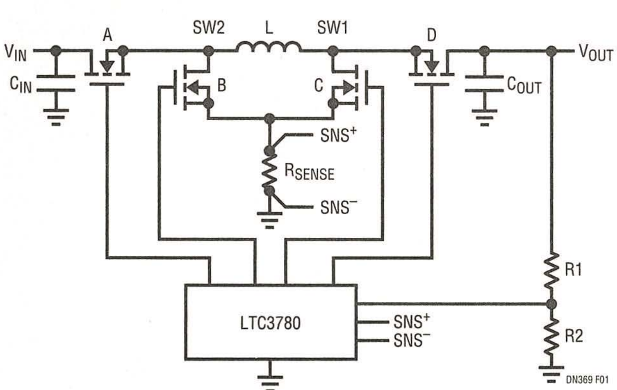

Figure 1. 4-Switch Buck-Boost Converter

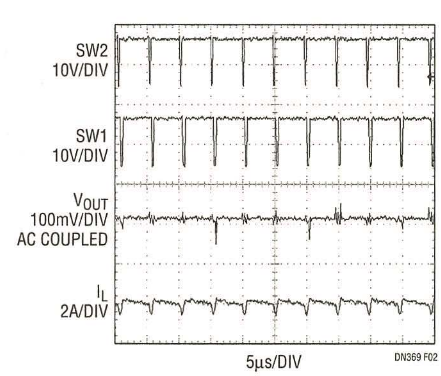

Figure 2. Switch Nodes and Inductor Current Waveforms (V_{IN} = V_{OUT} = 12V)

efficiency over a wide V_{IN} range. When the input and output voltages are both 12V, the 4-switch buck-boost has 99% efficiency at 2A load and 98% at its maximum 5A load (Figure 3). With its current mode control architecture, the converter has excellent load and line transition response, minimizing the required filter capacitance and simplifying loop compensation. As a result, very little filter capacitance is required. The single sense resistor structure dissipates little power (compared with multiple resistor sensing schemes) and provides consistent current information for short circuit and overcurrent protection.

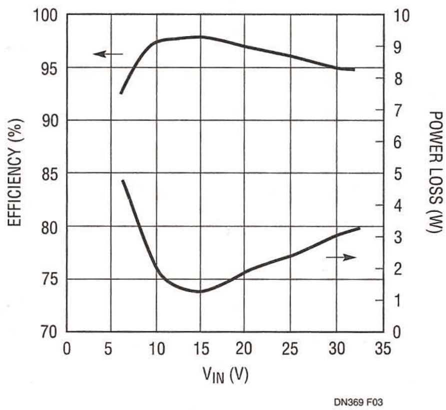

Figure 3. Efficiency and Power Loss (V_{OUT} = 12V, I_{LOAD} = 5A)

Replacing a SEPIC Converter

This single inductor buck-boost approach has high power density and high efficiency. Compared with a coupled inductor SEPIC converter, its efficiency can be 8% higher. Figure 4 shows the efficiency comparison between the LTC3780 4-switch buck-boost and a typical SEPIC converter. Note that a SEPIC converter has a maximum switch voltage equal to the input voltage plus the output voltage. So for a given maximum input voltage, a SEPIC would dictate the use of a higher voltage external switch than is required with the LTC3780. Moreover, the typical inductor occupies about 1/5th of a SEPIC transformer's footprint, less than 1/15th the volume and less than one-half the profile, as shown in Figure 5.

Protection for Boost Operation

The basic boost regulator topology provides no short circuit protection. When the output is pulled low, a large current can flow from the input to the output. Without

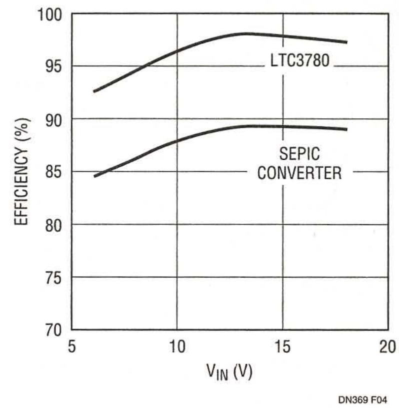

Figure 4. Efficiency Comparison Between the LTC3780 and a SEPIC Converter (V_{OUT} = 12V, I_{LOAD} = 5A)

shutting down the whole circuit, the LTC3780 circumvents this problem by forcing the converter into buck mode and using current foldback to limit the inductor current.

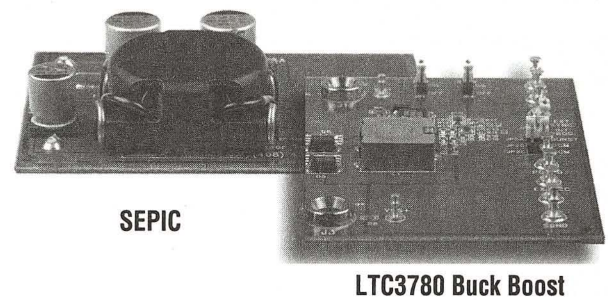

Figure 5. Inductor Size Comparison Between the LTC3780 5A/12V Converter (Right, 12.7mm × 12.7mm × 4mm) and a Typical SEPIC (Left, 21mm × 21mm × 10.8mm)

Simplify

For certain applications such as those requiring low current or not requiring current sinking, Switch D can be replaced with a Schottky diode. This simplified topology has approximately 2% lower efficiency.

Conclusion

The LTC3780 is a constant frequency current mode buck-boost switching regulator controller that allows the input voltage to be above, below or equal to the output voltage. Its high efficiency, high power density and single inductor topology make this product ideal for automotive, telecom, medical and battery-powered systems.

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Silicon Oscillators

High Performance Analog Solutions from Linear Technology

When was the last time you considered replacing a crystal oscillator with another clock device? In all likelihood, the answer is "never," and for good reason. After all, what performs like a crystal? The answer may surprise you.

At the heart of most clock circuits are crystal or ceramic resonators. These tried and true components boast excellent accuracy and stability, but their downside lies in their mechanical operation. As such, they are subject to wear-out, and physical impact can induce errors in the output frequency and phase. Vibration and temperature extremes can damage them and because they rely on a tuned circuit with a matched driver, they don't always start up as planned or oscillate at the intended frequency. Even the same device can start up differently from one power up cycle to the next.

An alternative to resonator-based clocks is RC-based clocks, which rely on the time-constant set by a resistor and capacitor. These are simple and more adjustable than fixed frequency crystal or ceramic devices, but poor accuracy and stability limit their usefulness.

Now there is another choice, a full family of silicon-based oscillators from Linear Technology.

A New Generation of Clock Devices

Just as vacuum tubes, relays and core memory were transformed by solid-state technology, silicon-based oscillators are beginning to displace traditional crystal and ceramic clock circuits. These devices do not rely on mechanical resonating elements and are not plagued by the poor performance of RC-based circuits. Standard silicon fabrication and assembly means inherent immunity to shock, vibration and wear-out. Start up is consistent and fast. In addition, these parts exhibit excellent accuracy, jitter, a small footprint, low power and operation from -40°C to 125°C. Linear Technology's oscillator family covers the frequency range from 1kHz to 170MHz, including both fixed and programmable frequency devices.

Fixed Frequency Alternative to Can-Type Oscillators

Linear's fixed frequency oscillators are simple, reliable, and robust devices. No trim components are required and these devices exhibit a maximum frequency error of +/-1% at 25ºC with stability of 20ppm/°C. Outstanding jitter, rise & fall time, and duty cycle provide an exceptionally "clean" square-wave. Typical start up time is 100µsec and an enable pin is provided for glitch-free control over the output. A divider pin allows division of the master clock frequency (÷1, ÷2, ÷4). Figure 1 shows the LTC®6905-133, which can generate an output frequency of 133MHz, 67MHz or 33.3MHz. Other available frequencies include 100MHz, 96MHz, 80MHz, 50MHz, 48MHz, 40MHz, 25MHz, 24MHz, and 20MHz.

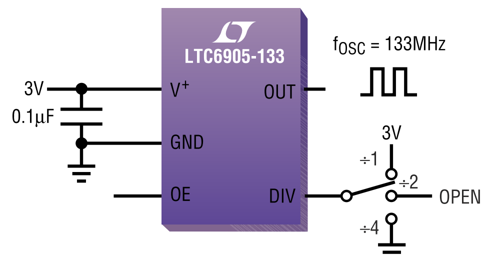
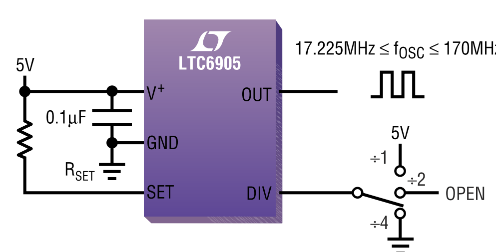


Figure 1. Fixed Frequency Silicon Oscillator

Any Frequency from 1kHz to 170MHz

Linear Technology offers two types of frequency programmable oscillators: resistor programmable and serial programmable. The frequency of a resistor programmable oscillator is set by a single external resistor (R_{SET}) and a pin-strapped divider. These devices can accurately generate a continuously variable frequency



$$f_{OSC} = \left(\frac{168.5\text{MHz} \bullet 10\text{k}\Omega}{R_{SET}} + 1.5\text{MHZ}\right) \bullet \frac{1}{N}, \quad N = \begin{cases} 1, \text{DIV Pin} = \text{V+} \\ 2, \text{DIV Pin} = \text{Open} \\ 4, \text{DIV Pin} = \text{GND} \end{cases}$$

$$10\text{k} \le R_{SET} \le 25\text{K}$$

Figure 2. Resistor Set Oscillators

Silicon Oscillators

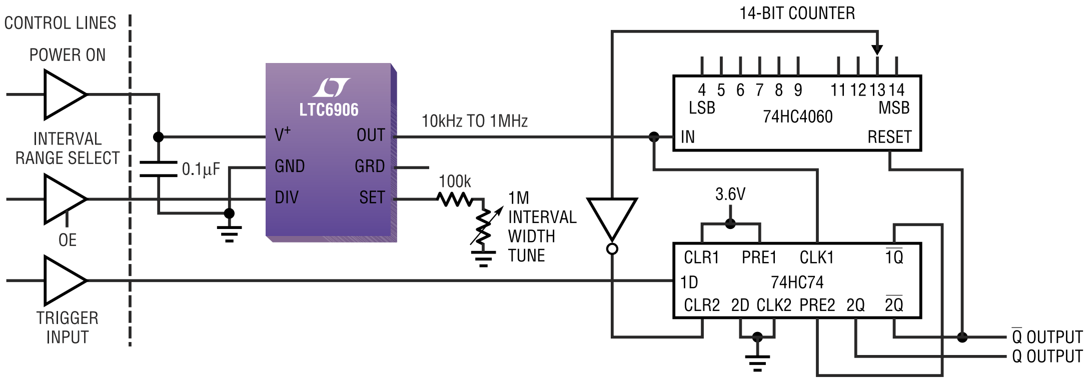


Figure 3. Micropower Tunable TIme Interval Generator

square wave without the use of a crystal, ceramic resonator or external clock reference. R_{SET} is chosen by a simple formula, shown in Figure 2.

The circuit is deceptively simple on the outside. Behind the curtain, however, a proprietary internal feedback loop works to maintain a precise relationship between R_{SET} and the output frequency, with a typical temperature coefficient of only 20ppm/°C and stability over the supply voltage range of 0.5%/V. Using a 0.1% resistor typically provides better than 0.6% accuracy from 0° to 70°C.

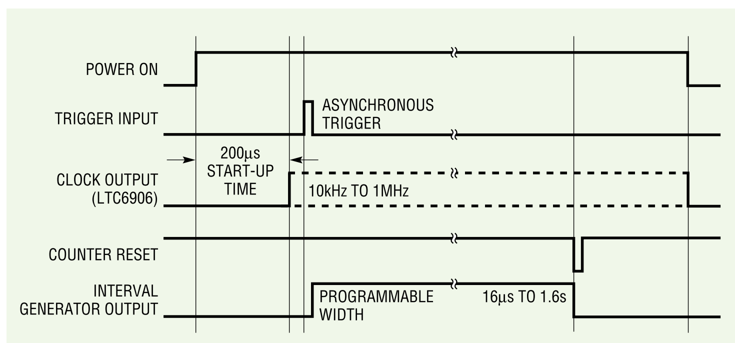


Figure 4. Timing Diagram for Time Interval Generator

Serial programmable oscillators are in many ways similar devices. The LTC6903/4 feature either an SPI or I^2C-compatible interface. Frequency can be set "on-the-fly" via an internal 10-bit DAC, with 4 additional bits to set the desired range, resulting in an output span of 1kHz to 68MHz with 0.1% resolution. Programming the frequency is simple, and no external components are required other than a bypass capacitor.

Applications

If you want to reduce power, you might want to take a second look at your clock. Consider the advantage of replacing your fixed frequency, power-hungry crystal device with a silicon oscillator that

Why Set the Frequency with a Resistor?

Infinite Frequency Resolution: One resistor sets ANY frequency in the oscillators operating range. This provides non-standard value reference clocks, such as those used in switched-capacitor filters. This adjustability also provides capability for adjustments late in the design cycle. Alternatively, this adjustment can be made during production calibration by using R_{SET} as a final trimmer.

Tiny Footprint: With a footprint as small as 9mm² and height of less than 1mm, these circuits are typically 5 to 10 times smaller than alternatives. With such a small solution, the oscillator can be placed right at the point of use, instead of routing fast clock signals over long distances.

Flexibility: Resistor programmable oscillators can be controlled via any method that sources current into the SET pin. This allows for voltage-controlled or current-controlled operation suitable for use in instrumentation (see Applications section).

Why Use a Programmable Silicon Oscillator?

Excellent Performance: Silicon oscillators combine stability over temperature (20ppm/°C) and supply voltage (0.5%/V) that far exceeds RC-based oscillators, while offering the tunability that crystals cannot achieve.

Shock, Humidity and EMI Immunity: Silicon oscillators have been tested to over 60,000 Gs without any measurable degradation in performance. Crystals, ceramic resonators and RC oscillators can also be sensitive to EMI as well as humidity.

Fast Start Up: Silicon oscillators power up quickly and predictably, typically within 100µsec. Crystals can take up to 10mS in the MHz range and up to a full second below 100kHz.

Low Power: Power consumption is directly related to the frequency of operation. This is true for crystal, RC and silicon oscillators. However, the power consumption of silicon oscillators at every frequency is 2 to 10 times lower than competing solutions.

Reduced Stocking: Since crystals and ceramic resonators operate at a fixed frequency, a separate part number is required for every frequency needed. Worse, a non-standard frequency could mean a high price and long lead-time. A single part number and some readily available resistors will solve this problem. Using the serially programmable devices, you don't even need the resistors.

can consume significantly less power and can be programmed to operate at different frequencies. As an example, the LTC6906, SOT23 micro-power oscillator consumes only 18µA max at 100kHz.

Viewing these devices for just power reduction, however, ignores their impressive flexibility as the following examples illustrate.

Micropower Tunable Time Interval Generator

An accurate, micropower time interval generator with large dynamic range and excellent stability appears in Figure 3. The circuit consists of a clock, a counter and a dual flip-flop. The LTC6906 silicon oscillator has an extremely low current draw and a fast start up, enabling a standard CMOS gate to awaken the circuit via the power supply pin. The output time interval pulse width is set by the oscillator's frequency and the counter's modulo. As shown, the interval is programmable from 16 µsecs to 1.6 seconds, and additional counters can extend this range. 100ppm stability is achievable over temperature by combining 50ppm resistors with the 50ppm stability of the LTC6906. By powering off the clock

Table 1. Complete Family of SIlicon Oscillators

	Device	Frequency Output	Accuracy (Max 25°C)	Supply Current	Drift	Package	Notes
Fixed Frequency	LTC6905-135	133, 67.7, or 33.3MHz	1%	10mA @133MHz	20ppm/°C	SOT23-5	No trim components required, divide by 1, 2, or 4, output enable-provided 100µs startup time 50ps jitter
	LTC6905-100	100, 50, or 25MHz		8mA @100MHz			
	LTC6905-96	96, 48, or 20MHz		8mA @96MHz			
	LTC6905-80	80, 40, or 20MHz		7mA @80MHz			
Resistor Set	LTC1799	1kHz to 33MHz	1.50%	1mA @3MHz	40ppm/°C	SOT23-5	Wide frequency range
	LTC6900	1kHz to 20MHz	1.50%	500µA @3MHz	40ppm/°C		Low power, 50µsec startup
	LTC6902	5kHz to 20MHz	1.50%	700µA @3MHz	40ppm/°C	MS-10	Spread spectrum with 1, 3 or 4 phase outputs
	LTC6905	17MHz to 170MHz	1.40%	7mA @170MHz	20ppm/°C	SOT23-5	High frequency, 100µsec startup, 50psec jitter, w/ divide by 1, 2 or 4
	LTC6906	10kHz to 1MHz	0.50%	60µA @1MHz	50ppm/°C	SOT23-6	Micropower, no bypass cap
Serial I/F	LTC6903	1kHz to 68MHz (0.1% Resolution)	1.10%	1.7mA @3MHz	10ppm/°C	MS-8	I^2C interface, w/ output enable No trim components required
	LTC6904						SPI interface, w/ output enable No trim components required

LINEAR TECHNOLOGY

Silicon Oscillators

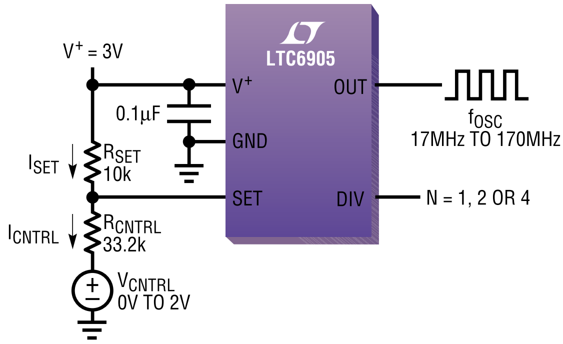


Figure 5. VCO Operation Using the LTC6905

when not needed, the current draw is reduced to the quiescent current of the CMOS flip flop and counter.

WIde Range, Linear VCO

Frequency can be set with Linear Technology's resistor programmable oscillators via any method that sources current into the SET pin. This is particularly useful for the LTC6905 with a wide frequency range of 17MHz to 170MHz. Figure 5 shows the use of a voltage source to control frequency. The R_{SET} resister establishes a constant current into the SET pin, and the current through R_{CNTRL} will subtract from this current to change the frequency. Thus, increasing V_{CNTRL} increases the output frequency. Figure 6 shows the wide frequency range and excellent linearity that can be achieved with this simple technique.

Remote Sensing

Replacing R_{SET} with a resistive-based sensor, such as a thermistor, allows for direct conversion of a sensor output into frequency. In Figure 7, a thermistor is used for a simple temperature-to-frequency generator. By conversion to a digital signal (the CMOS clock output), measurements can be taken remotely and transmitted digitally. An opto-isolator can then be used to electrically isolate the sensor and avoid ground loops. Adding series and parallel resistors for specific thermistors and temperature ranges can improve linearity. Because the resistor programmable oscillators have a small footprint, wide operating range, and low drift, they can be used in this application directly at the point of measurement with minimal design impact.

Microcontroller Applications

Programmable silicon oscillators are also an excellent solution as a microprocessor master clock. For speeds up to 170MHz, these devices provide a stable, flexible clock signal - especially useful if the processor must run at multiple frequencies (such as for sleep and standby). Using either an SPI or I²C-compatible serial interface, the CPU can program its own clock for each mode. Using any of the other Linear Technology oscillators, the frequency can be easily "throttled-back" using the DIV pin. This allows the microcontroller to reduce system power when high-speed operation is not necessary.

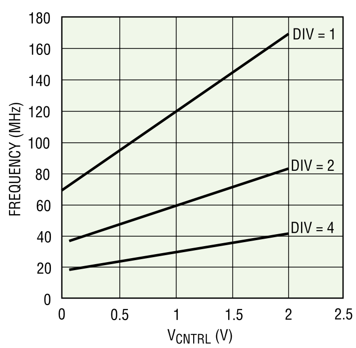


Figure 6. VCO Frequency vs. Voltage at Various Divider Settings

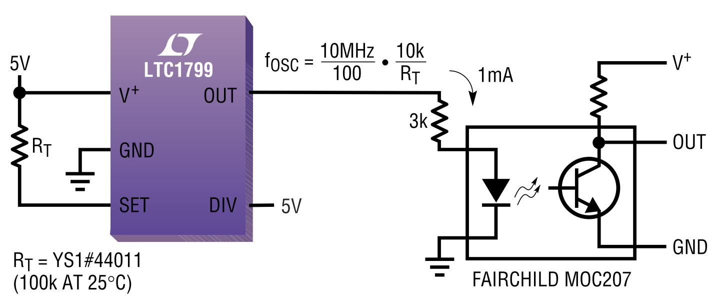


Figure 7. Remote Thermal Sensor Using a Thermistor

BY DAVID CALDWELL • FLEXTEK ELECTRONICS

Power goes digital

DESIGNERS LACK SIMPLE TOOLS TO SQUEEZE PERFORMANCE OUT OF MICROCONTROLLERS IN POWER CONVERTERS. EASY-TO-UNDERSTAND GUIDELINES CAN HELP DESIGNERS TAKE ADVANTAGE OF ANALOG KNOWLEDGE TO EASE THE TRANSITION INTO DIGITAL CONTROL FOR POWER DESIGNS.

Power-design engineers are starting to use digital control in power converters, but the transition has been slow and limited. Many power designers erroneously believe that only high-end systems justify the burden of DSP chips and that simple microcontrollers lack the throughput necessary for reasonable performance in common converters. In reality, the biggest obstacle to technological growth has been that digital and analog designers speak different languages, which hampers progress.

A typical design session for a digitally controlled converter starts with a power engineer sizing the output LC filter based on switching frequency and a firmware engineer writing microcontroller code to adjust the output as a function of measured voltage. After guessing control gains and failing to achieve a fast stable voltage response, the engineer deems the microcontroller inadequate, and a DSP is too expensive and power-hungry for this simple application.

However, engineers cannot completely independently write filter-selection and feedback-control code: They must modify analog-design rules for sizing filters to accommodate processing and update delays in digital controllers, and they must streamline firmware algorithms from motion control to run quickly enough to keep the filter from ringing. Once engineers identify and understand the critical issues, optimization tends to flow naturally.

All engineers understand a scope trace, but few are comfortable going back and forth from time domain to S and Z domains, so the resulting trial-and-error responses tend to be disappointing. Engineers require some simple tools and guidelines from multiple disciplines that they can easily understand and apply.

DESIGN EXAMPLE

The buck converter in **Figure 1** has an inexpensive 8-bit PIC16F818 microcontroller with slow A/D conversion and no hardware multiplier. Using a simple microcontroller illustrates universal digital-power-design concepts, and it's easier to port code to a higher capability device than to do the reverse.

The PIC16F818 has an ADC to measure output voltage and a PWM to adjust the duty cycle of the integrated half-bridge power-stage TDA21201. The output voltage for this synchronous rectifier is the input voltage scaled by the ratio of high time

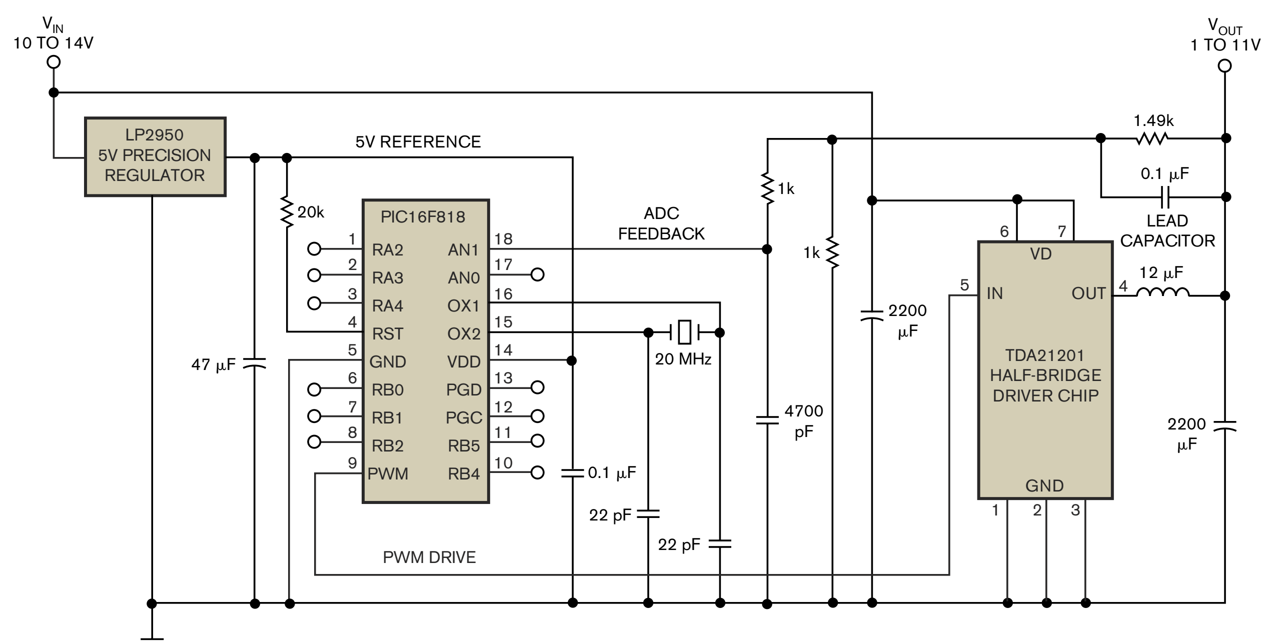


Figure 1 This buck converter has an 8-bit PIC16F818 microcontroller with slow A/D conversion and no hardware multiplier.

to the total switching period, smoothed by the LC filter (**Figure 2**). The control algorithm that calculates PWM drive to obtain the desired ADC voltage is PID (proportional-integral differential). It repeatedly adjusts duty cycle to maintain a fast stable output voltage in response to load and input variations.

The converter is an 80W (1 to $11V_{OUT}$ at 7.3A) nonisolated buck converter, whose total parts cost less than $8 based on distributor prices—hence, the name, "8-buck converter." Key performance parameters include 92% efficiency and 12-mV rms ripple at a 156-kHz switching frequency. The microcontroller has a 20-MHz clock and performs PID-control updates every 25.6 μsec. **Figure 3** illustrates the closed-loop transient response of the converter to a 3A step load, which is comparable with that of common converters with analog-control loops. This example takes the open-loop response at a fixed duty cycle (PID gains at zero) to illustrate how a properly implemented PID loop quickly compensates for voltage droop without ringing.

Although this converter offers the opportunity for firmware customization, designers must accept that digital control adds delays that may impact converter performance. Given the same switching frequency, a converter with a digital-control loop has a lower bandwidth than its analog counterpart, so a larger inductor and capacitor may be necessary in the filter. The converter bandwidth must exceed the resonant frequency of the filter to preclude ringing, so select the LC time constant for controllability.

The effective lag in a digital-control loop is the combination of two effects: processing delay and update interval. Processing delay is the time it takes to convert analog feedback to digital, process the control-algorithm calculations, and then adjust output drive. Update interval is the time between adjustments of output drive. These terms define how often (update interval) the system corrects and how old (processing delay) the information is that the correction used.

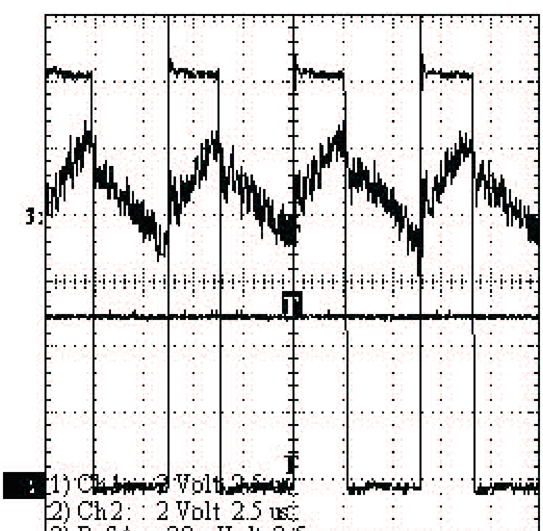


Figure 2 The converter waveforms show that the output voltage is the average of the switching-power-stage values. Waveform 1 is the switching-power stage (2V/div, 2.5 μsec/div). Waveform 2 is the filtered output voltage (2V/div, 2.5 μsec/div). Waveform 3 is the output-voltage ripple (20 mV/div, 2.5 μsec/div).

Although tools are available to precisely analyze mixed-signal systems, they tend to be somewhat costly and specialized and do not promote an intuitive understanding of critical concepts. To make digital-power control accessible to the most people, this article uses the following analog equivalent based on reasonable approximations. The resultant circuit is simple enough to run on evaluation versions of Spice. Engineers can then take advantage of decades of analog knowledge in the power field to promote greater understanding of digital control.

ANALOG EQUIVALENT

The first step in creating an analog equivalent of a switching converter with digital control is to average the power stage. Averaging is valid because the switching frequency is much higher than the LC-filter resonance. You then perform a similar averaging process with the PID-control algorithm and associated delays. RC networks simulate the processing and update delays. This imprecise approximation is reasonable and effective, and multiple hardware cases validate it.

Figure 4 shows the Spice equivalent of the 8-buck converter in **Figure 1**. You can step the I_{LOAD} independent current source or V_{REF} voltage source in the time domain to capture the closed-loop transient response at the V_{OUT} test point.

The 2.4 gain for the switching-averaged model of the power stage, ESWAVG, is the ratio of the nominal 12V input voltage to the 5V range of the PWM command. This example uses measured values for LC components and equivalent series resistances for improved accuracy and increases R_L to approximate switch and pc-board resistance. This scenario added the 0.1-μF lead capacitor in the ADC resistive-divider network after initial simulations indicated it could improve transient performance.

The microcontroller calculates the PID-control loop in firmware every update interval as follows:

- $V_{ERR}=V_{REF}-V_{ADC}$; error=setpoint−measured.

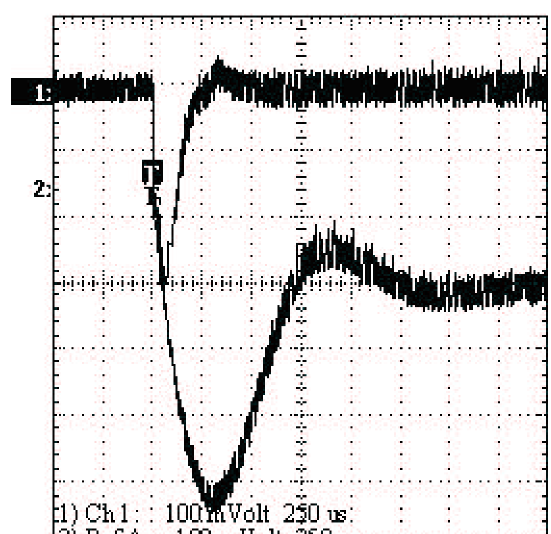


Figure 3 Waveform 1 is the closed-loop transient response to a 3A step load that compares with common analog converters. Waveform 2 is the open-loop response that illustrates the benefit of digital control.

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# of Outputs	Device	Regulators PWMs	Regulators Linears	Int. FETs	V_{IN} (V)	I_{OUT} (max) (A)	Package
4	ISL6521	1	3		5	20	SOIC-16
3	ISL6455	1	2	✓	3.3	0.6	QFN-24
	ISL6455A	1	2	✓	5	0.6	QFN-24
	ISL6537	2	2 + Ref		2.5, 12	20	QFN-28
	ISL6532A	1	2		5, 12	20	QFN-28
	ISL6441	2	1		4.5 to 24	6	QFN-28
	ISL6443	2	1		4.5 to 24	10	QFN-28
2	ISL6227	2	0		4.5 to 24	16	SSOP-28
	ISL6440	2	0		4.5 to 24	10	QSOP-24
	ISL6539	2	0		5 to 15	8	SSOP-28
	ISL6530/1	2	Ref		5	1	SOIC-24, QFN-32
	ISL6528	1	1		3.3, 5	15	SOIC-8
	ISL6529	1	1		3.3 to 5, 12	15	SOIC-14, QFN-16

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- $V_{ERRDIFF}=V_{ERR}-V_{ERRLAST}$; differential error between samples.
- $V_{ERRLAST}=V_{ERR}$; save current error for next differential calculation.
- $P=K_P\times V_{ERR}$; K_P=proportional gain=4 in 8-buck code.
- $I=I+K_I\times V_{ERR}$; K_I=integral gain=0.25 in 8-buck code.
- $D=K_D\times V_{ERRDIFF}$; K_D=diifferential gain=4 in 8-buck code.
- PWM=PID=P+I+D; make PWM-output adjustment.

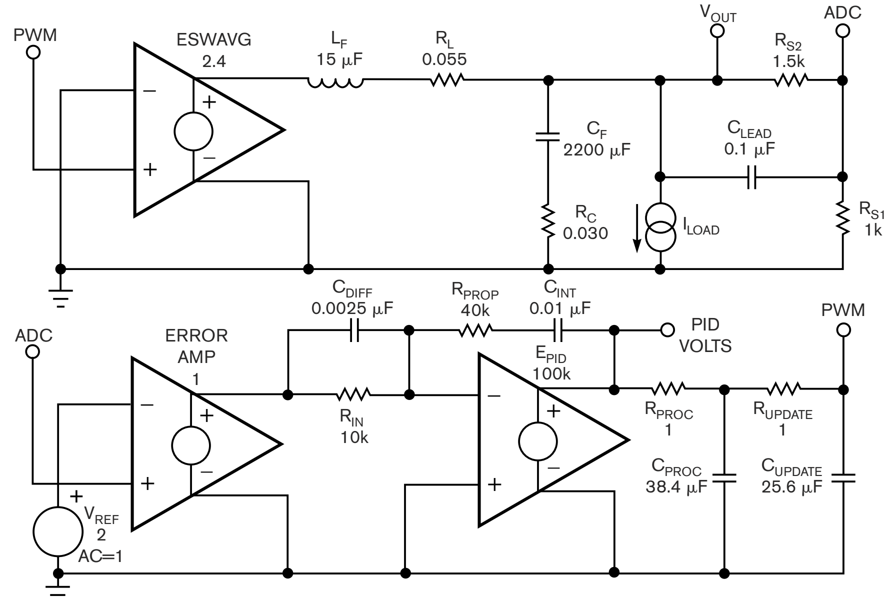
PID gain terms K_P, K_I, and K_D are ratios of the most significant bit of PWM to ADC values in microfirmware.

The EPID op amp simulates the PID firmware in the Spice circuit with the following RC components:

- Select R_{IN}=10K.
- $R_{PROP}=K_P\times R_{IN}=4\times 10K=$ 40K.
- $C_{INT}=T_{UPDATE}/(K_I\times R_{IN})=$ 25.6 μsec/(0.25×10K)×0.01 μF.
- $C_{DIFF}=K_D\times T_{UPDATE}/R_{PROP}=$ 4×25.6 μsec 40K×0.0025 μF.

T_{UPDATE} is the 25.6-μsec update interval of the microcontroller, whose associated delay R_{UPDATE} and C_{UPDATE} simulate. The 38-μsec processing delay is the sum of the A/D-conversion time, 19.2 μsec, and the PID-calculation time, 19.2 μsec, rounded up to the next interval of the switching period, 6.4 μsec.

You measure loop gain and phase margin at the ADC symbol after the power stage by sweeping V_{REF} in the frequency domain. You must first break the feedback loop by removing the ADC symbol from the error amp and connecting V_{REF} to the noninverting input of the error amp with the inverting input grounded. **Figure 5** shows the loop-gain Bode plot, which indicates 2.4-kHz control bandwidth (frequency at unity gain, or 0 dB) with 45° phase margin (phase at unity-gain frequency).



NOTE: ESWAVG IS THE GAIN FOR THE SWITCHING-AVERAGED MODEL OF THE POWER STAGE.

Figure 4 The 8-buck converter of Figure 1 has an analog Spice equivalent.

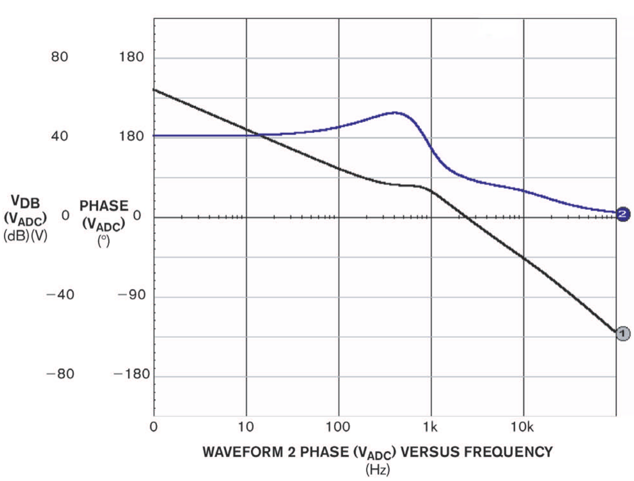


Figure 5 The control-loop gain indicates 2.4-kHz bandwidth and a 45° phase margin.

One limitation of the analog model is that it allows greater differential compensation than is possible in digital hardware. Phase lead requires a prediction based on the recent past that is invalid with old data, so processing and update delays limit the gain term, K_D. Excessive differential gain appears in hardware as nonlinear ringing and extended envelope to a stepped load, in contrast to the sinusoidal ring and exponential decay of a linear system. The simulation determined the lead capacitor in the feedback network of **Figure 1** to compensate for this effect.

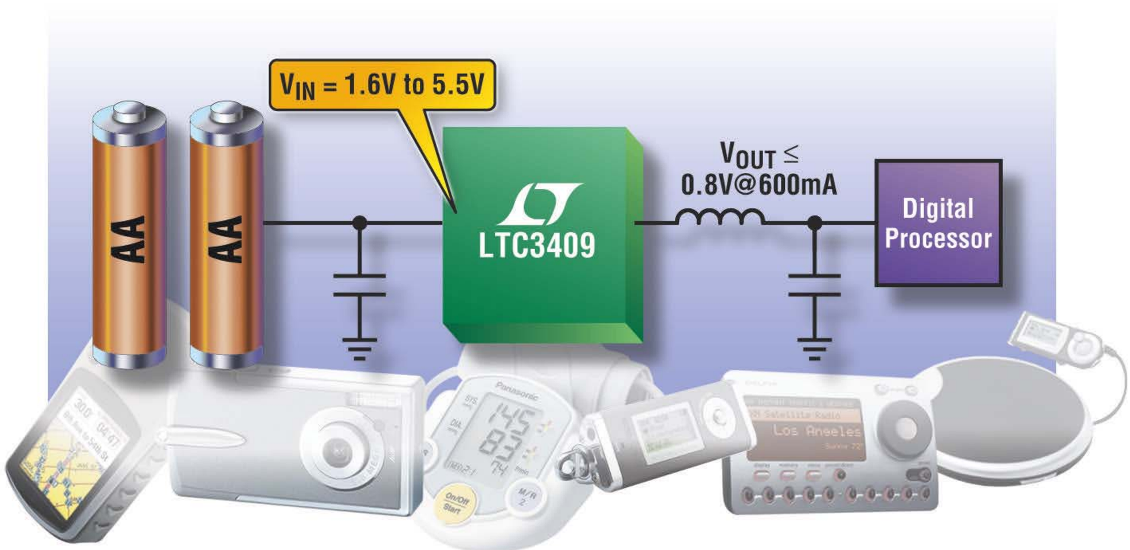
In general, the compensator cannot achieve more than 45° lead within the bandwidth of the control loop, so check that the phase at test point PID is less than 225° (inverting loop is initially 180°) at the unity-gain frequency of the entire loop. If the phase exceeds this limit, then accept lower gain and bandwidth or add analog lead to the circuit. The basis of this design guideline comes from the control bandwidth having a direct relationship to the digital delays that limit differential gain.

DESIGN GUIDELINES

The real value of this model is the intuitive understanding that it provides and the ability to take advantage of a designer's knowledge of traditional power converters. For example, rules of thumb say that the control bandwidth must be at least four times lower than the switching frequency. Most loops are closer to a decade below the switching frequency, so 6.3 is a reasonable goal, because it is halfway between 4 and 10 on a log scale. However, anyone who has used a microcontroller to control a power converter finds that this goal is nearly impossible to accomplish. The update interval of the control loop is usually slower than the switching frequency, and you must also consider the additional delays of processing the ADC and PID, which leads to the first two guidelines in the **sidebar**, "Design guidelines for digital-power control."

Once you bound the control bandwidth for a digital converter,

2 AA Buck Regulator



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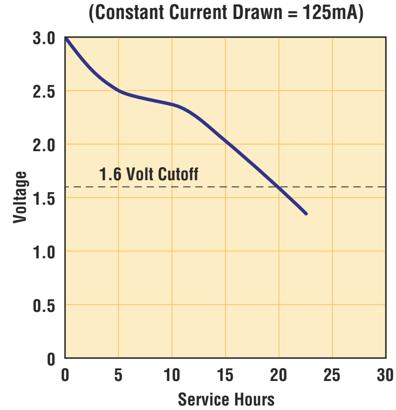
- 8-Lead 3mm x 3mm x 0.75mm DFN package

Discharge Profile of 2 AA Cells
(Constant Current Drawn = 125mA)



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LINEAR TECHNOLOGY

you can then approximate the LC resonant frequency because it must be within the control bandwidth. The **sidebar**'s **Guideline 3** assumes that the LC frequency is no more than half the control bandwidth, which is 6.3 times less than the critical frequency. (The 6.3 cancels 2π in the LC equation.) **Guideline 3** is an additional design constraint beyond traditional efforts to limit switching ripple.

PWM resolution alone does not limit the switching frequency of a digital converter. Effective control resolution can be significantly higher than PWM resolution because multiple PWM corrections take place within the time constant of the LC filter. Additionally, effective control resolution can be higher than ADC resolution because you integrate multiple readings, and inherent switching noise acts as averaging dither. However, quantization ripple (sometimes incorrectly referred to as "limit cycling") may occur as the output voltage varies between two neighboring ADC levels (least significant bits), because the filter time constant is usually insufficient to mask oversampling. **Guideline 4** in the **sidebar** covers PWM-frequency selection to balance ripple and resolution.

Despite the precise appearance of these equations, the guidelines are based on approximations that users can adjust. For example, the design exceeded the calculated PWM limit to round up to the nearest power of two, based on the 20-MHz microcontroller clock. Some tweaking may occur based on hardware performance, but the guidelines provide a reasonable starting point and strong advantage over trial-and-error approaches.

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APPLICATIONS AND TRENDS

Understanding and knowledge enable designers to make effective trade-offs and accelerate development. The design guidelines of the **sidebar** can help you decide whether the custom features of a digitally controlled power converter justify lower performance with a microcontroller, or added cost, power, and complexity with a DSP. The latest technology is not always the greatest, so analog may still be the better choice, depending on system requirements.

You can apply the Spice model to estimate hardware-component values and firmware parameters before building and testing. You can use it for control applications in virtually any field, including power, thermal, motion, lighting, and flow. Measure the system's open-loop step response, then adjust the model to match gain (ESWAVG) and timing (LC filter). Make RL impedance large relative to LF for a single-pole system and C_{PROC} and C_{UPDATE} negligible for an analog controller.

These tools do not address the critical task of firmware development, which opens the front door to innovation and a trap door to disaster. When I published **Reference 1** in 1998 with a vision statement for the future of digital-power control, the industry expected that many tasks would be automated by now. However, designers largely face the same choice they had many years ago: Apply a limited device, or design from scratch.

Semiconductor companies continue to crank out countless variations of application-specific chips and a few "placebo" devices that let designers feel state of the art without enabling new and useful capabilities. Components are necessary to automate challenging control tasks and to enable easy customization. Until then, designers must painstakingly manage their own designs. **Reference 2** provides additional details, including useful short cuts and tips to avoid common pitfalls in digital-power control.

Power converters may be the most common electronic subsystems in the world, but they still lag other products in technological advancements. Understanding key concepts is essential in satisfying the growing demands and constraints on the power industry. With any luck, these guidelines and tools will aid in that effort. EDN

DESIGN GUIDELINES FOR DIGITAL-POWER CONTROL

GUIDELINE 1: CRITICAL FREQUENCY

$f(critical)=1/[T_{PROCESS}+T_{UPDATE}]=1/[(T_{ADC}+T_{PID})+T_{UPDATE}]$.

In the 8-buck example, $1/[(19.2\ \mu sec+19.2\ \mu sec)+25.6\ \mu sec]$=15.6-kHz limit<<156-kHz switching.

Comment: Digital delays rather than switching frequency limit converter performance.

GUIDELINE 2: CONTROL BANDWIDTH

f(control)<f(critical)/4. (Factor of 4 is the limit, 10 is common, and 6.3 is the goal.)

In the 8-buck example, 15.6 kHz/6.3=2.5 kHz (close to the 2.4-kHz simulation result).

Comment: Critical frequency bounds control-loop bandwidth.

GUIDELINE 3: LC FILTER

$LC^{1/2}>2/f(critical)=2/15.6\ kHz=128\ \mu sec$.

In the 8-buck example, $[12\ \mu H\times 2200\ \mu F]^{1/2}=162\ \mu sec>128\ \mu sec$ (satisfied in design).

Comment: Contain the LC-filter resonance within the loop bandwidth.

GUIDELINE 4: PWM FREQUENCY

$f(PWM)<[f(CLK)/2^{RES(ADC)}]\times[LC^{1/2}/T_{UPDATE}]\times[V_{MEAS}/V_{IN}]$.

In the 8-buck example, $f(CLK)/2^{RES(ADC)}=20M/2^{10}=19.5$ kHz (PWM frequency to match 10-bit-ADC resolution).

$LC^{1/2}/T_{UPDATE}=162\ \mu sec/25.6\ \mu sec=6.3$ (PWM adjustments within the filter time constant).

$V_{MEAS}/V_{IN}=[5\times(1\ k\Omega+1.5\ k\Omega)/1\ k\Omega]/12=1.04$ (voltage ratio measurable by ADC).

$f(PWM)<19.5\ kHz\times 6.3\times 1.04=128$ kHz (rounded up to 156 kHz in design).

Comment: Maximum PWM frequency with control resolution is equal to ADC.

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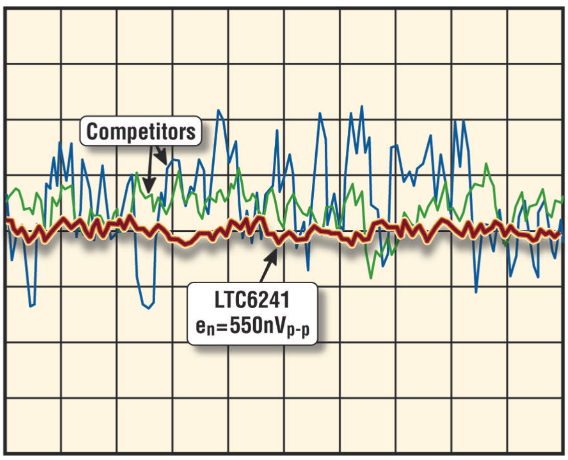
AUTHOR'S BIOGRAPHY

David Caldwell founded Flextek Electronics in 1996 to advance digital-power control. He has an MSEE and 20 years' experience, has published more than a dozen papers, and holds two patents. He has taught professional courses in digital-power control.

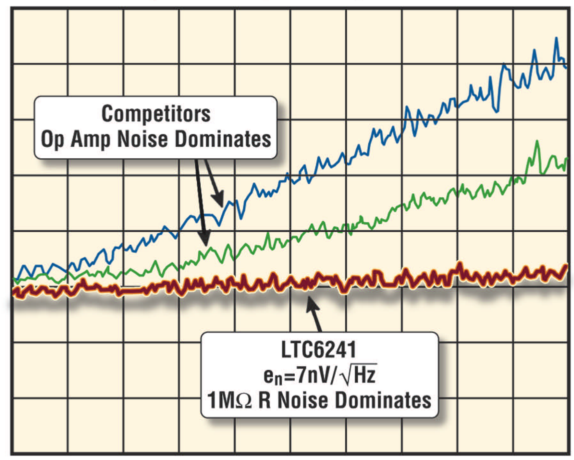
Low Noise CMOS

Low Frequency Noise

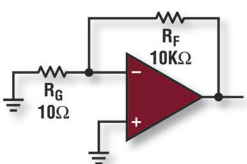


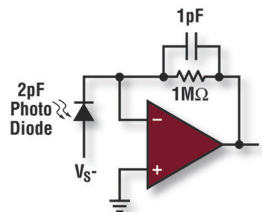
0.1Hz to 10Hz Input Referred Noise

High Frequency Noise



1kHz to 100kHz Noise Voltage Density





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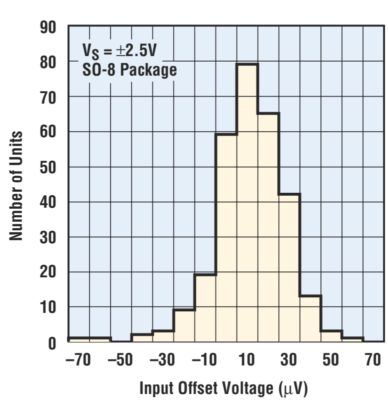

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READERS SOLVE DESIGN PROBLEMS

DIs Inside

Build a precise dc floating-current source

D Ramírez, S Casans, C Reig, AE Navarro, and J Sánchez, University of Valencia, Burjassot, Spain

Although well-known to active-filter theorists and designers, GICs (generalized impedance converters) may be less familiar to analog generalists. Comprising a one-port active circuit typically comprising low-cost operational amplifiers, resistors, and capacitors, a GIC transforms capacitive reactance into inductive reactance and thus can substitute for an inductor in a filter that an RLC-transfer function describes. In addition, the flexibility of a GIC's input-impedance equation permits the design of virtual impedances that don't exist as physical components—for example, frequency-dependent resistance (**Reference 1**). The GIC, which its developers introduced 30 years ago, has seen its greatest application in ac-circuit and active-filter applications.

Figure 1 shows a classic GIC circuit in which the input impedance, Z_{IN}, depends on the nature of impedances Z_1 through Z_5. The following equation describes the circuit's input impedance:

$$Z_{IN}=\frac{V_{IN}}{I_{IN}}=\frac{Z_1\times Z_3\times Z_5}{Z_2\times Z_4}.$$

For example, if Z_1, Z_2, Z_3, and Z_5 comprise resistors R_1, R_2, R_3, and R_5, and Z_4 comprises capacitor C_4, then the input impedance, Z_{IN}, appears as a virtual inductor of value L_{IN}:

$$L_{IN}=\frac{R_1\times R_3\times R_5\times C_4}{R_2}.$$

Figure 2 shows the GIC circuit in its dc configuration. When you consider the GIC circuit in a purely dc environment, you can envision new applications. For example, you could replace impedances Z_1 through Z_5 with pure resistances R_1 through R_5. Instead of an ac input-voltage source, connect a precision temperature- and time-stable dc reference voltage to the input port. A simple circuit analysis using ideal op amps for IC_1 and IC_2 shows that the reference input voltage, V_{REF}, appears across resistor R_5, and, as the following equation shows, a constant current, I_O, flows through R_5.

$$I_O=\frac{V_{REF}}{R_5}.$$

However, op amp IC_2's noninverting input diverts a small amount of current from the junction of R_4 and R_5, and I_O thus also flows through R_4. Selecting

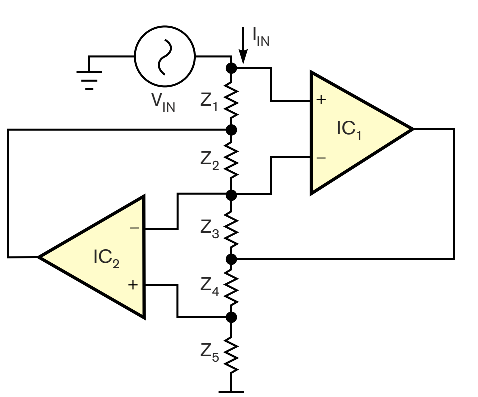

Figure 1 A classic generalized impedance converter provides a single-port impedance that appears at V_{IN}. The schematic omits power connections for clarity.

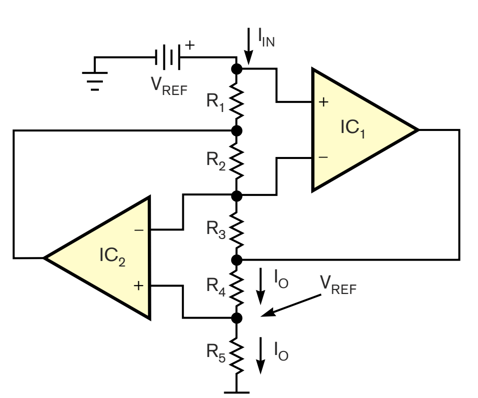

Figure 2 Replacing all of a GIC's impedances with resistors creates a constant-current source.

large values for R_1, R_2, and R_3 helps minimize current drawn from the reference voltage. For example, the circuit can supply 2 to 10 mA to R_4 and draw only a few tenths of a microampere from the reference source. Using tight-tolerance and low-drift components for V_{REF} and R_5 ensures the stability of I_O. Applications include providing constant-current drive for Wheatstone-bridge and platinum-element sensors (**Reference 2**). In addition, you can replace R_4 with a series of resistive sensors as in an Anderson loop (**Reference 3**).EDN

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3. Anderson, KF, "Looking under the (Wheatstone) bridge," *Sensors*, June 2001, pg 105.

Frequency dithering enhances high-performance ADCs

Steve Hageman, Windsor, CA

Since the late 1970s, designers have successfully improved the effective resolution and spurious performance of A/D converters by adding dither—uncorrelated noise—to a converter's input and then using DSP techniques to average out noise from the converted data. The most common dithering method adds random-amplitude noise to an A/D converter's input signal. Although this method works, the added noise includes large random peak values. To keep the A/D converter's input out of the saturation region, a designer must know both the peak signal and the peak dither levels. Even briefly saturating the A/D converter adds more nonlinearities than dither can remove.

Another approach adds a dithered-frequency, constant-amplitude signal. **Figure 1** shows one possible implementation featuring a Linear LTC1799 programmable oscillator, IC_2, that's operated in a VCO (voltage-controlled-oscillator) mode in which an applied voltage modulates the center frequency. You can set the LTC1799's center frequency at 1 kHz to 33 MHz, making it a suitable dither generator for many currently available A/D converters. Because the LTC1799's output comprises a square wave, its peak output amplitude is well-defined.

You can set the random-dither center frequency either below or above the signal frequency of interest. For conversion of a narrowband intermediate frequency, either location may work well. For an A/D converter that must operate to dc, the only useful location is above the signal frequency of interest. One approach places the dither frequency at one-half of the sampling or the Nyquist frequency. When you place it there, the random noise typically doesn't interfere with the desired signal, and any aliasing that occurs only folds the random frequency noise around itself and not into the desired signal band.

The circuit in **Figure 1** operates with a 20-MHz sampling A/D converter and generates random noise around a center frequency of 10 MHz. You can use any of a number of techniques to generate the random noise, including dig-

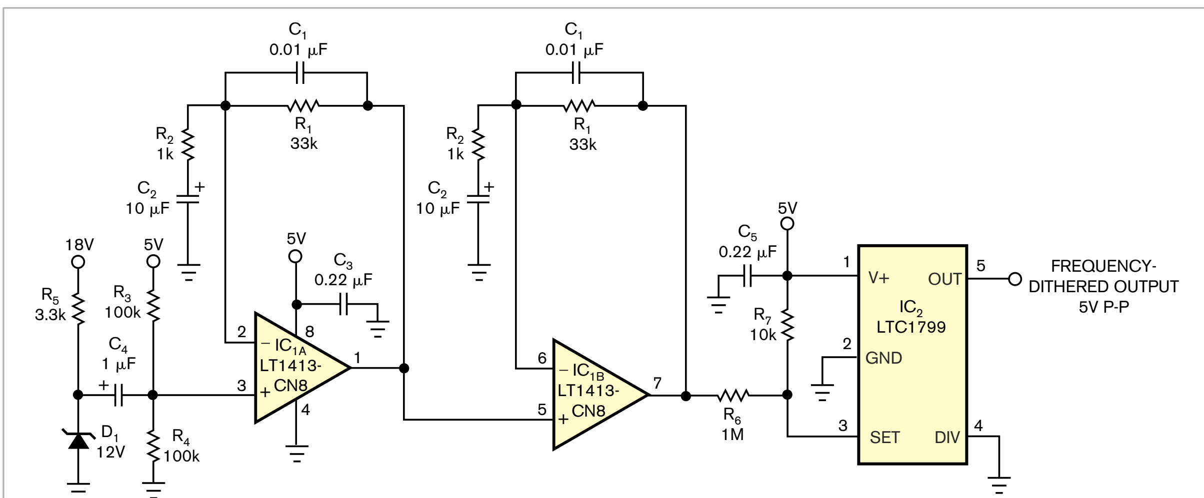


Figure 1 A zener diode, two stages of amplification, and an FM voltage-controlled oscillator form a constant-amplitude dither generator.

ital shift registers and semiconductor junctions biased into the breakdown range. In this design, a 12V zener diode, D_1, generates the noise, which a two-stage amplifier amplifies and frequency-shapes. If necessary, you can further shape the noise distribution by using more complex active-filter sections, IC_{1A} and IC_{1B}. After filtering, the noise modulates the LTC1799. Make sure that the LTC1799's power-supply voltage is pure dc and free of ripple, because power-supply noise produces nonrandom AM sidebands.

Figure 2 shows an amplitude-versus-frequency plot of the frequency-limited spectrum that the design in **Figure 1** produces. Depending on the circuit's configuration, you can apply the dither to the A/D converter using a small coupling capacitor or a more complex active summing circuit. Although zener-diode noise generators offer theoretical simplicity, they behave poorly in production environments because their noise outputs can vary greatly. Even among diodes from the same manufacturing batch, you can observe popcorn noise, unevenly distributed noise histograms, amplitude shifts, and frequency-weighted noise. In a high-volume application, well-specified noise diodes, such as those from Micronetics (www.micronetics.com), may prove more cost-effective than zener diodes.

Once you select a noise diode, you can select amplification-stage gains such that clipping of noise peaks isn't evident at the circuit's output. If your application requires it, you can alter the amplifiers' frequency responses to alter the noise spectrum. Finally, adjust the LTC1799's frequency-setting resistors, R_6 and R_7, so that the noise-spectrum display resembles that in **Figure 2**. Any clipping along the amplifier path tends to add peaks to the edges of the spectrum, which indicates amplitude clipping and reduction of the noise's random characteristics.

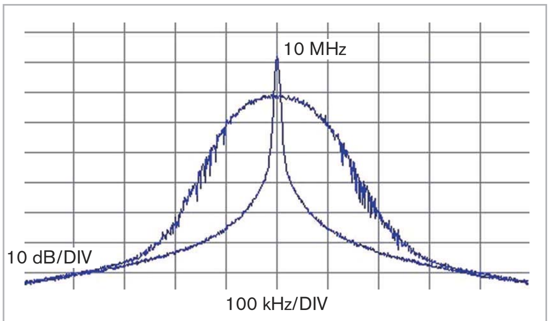


Figure 2 The broad bell-shaped curve shows a random-frequency-dithered spectrum superimposed onto the LTC1799's unmodulated, 10-MHz output.

You can add a filter between the noise output and the A/D converter's summing input to limit inband noise or remove any periodic modulation that power-supply ripple introduces. In a modern, high-performance A/D converter, even a small amount of periodic noise can manifest itself as a −80-dBc (decibels-below-carrier) spurious response. EDN

Memory-termination IC balances charges on series capacitors

Clayton B Grantham, National Semiconductor, Tucson, AZ

As one of today's most interesting component families, high-value capacitors offer ratings ranging from tenths to tens of farads but suffer from relatively low working voltages. For example, Maxwell's (www.maxwell.com) PC10 ultracapacitor occupies an area about the size of a large postage stamp and the thickness of four stacked US 25-cent coins. The PC10 provides 10F capacitance, a 2.5A maximum discharge-current rating, and an 18Ω ESR (equivalent-series resistance). However, its rated working voltage is only 2.5V.

To accommodate a supply voltage greater than 2.5V, you can connect two capacitors in series, halving the available capacitance and doubling the overall voltage rating. However, due to differences in leakage current and capacitance, the voltage at the capacitor's common connection can vary, and your design must ensure that you do not exceed either capacitor's maximum voltage rating. If the series-connected capacitors' charge and discharge currents are relatively small, you can connect equal-valued charge-balancing resistors across both capacitors. But for farad-range capacitors that can deliver amperes of current, you need a more efficient approach.

The theoretical voltage across a capacitor comprises its initial voltage, $V_C(0)$, plus the integral of the capacitance, C, multiplied by the capacitor's current over time: $V_C(t)=V_C(0)+C\times\int I(t)dt$. In a two-capacitor divider, the current through both capacitors is

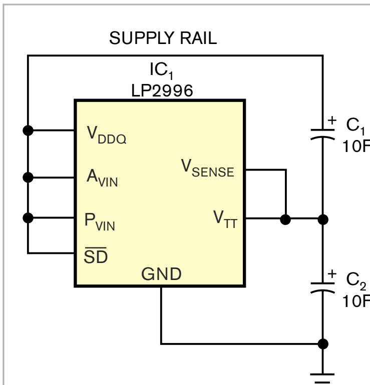
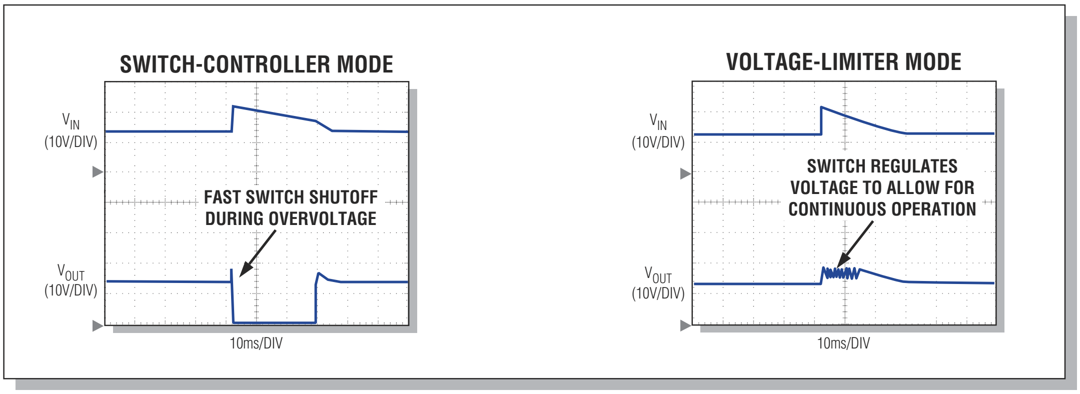
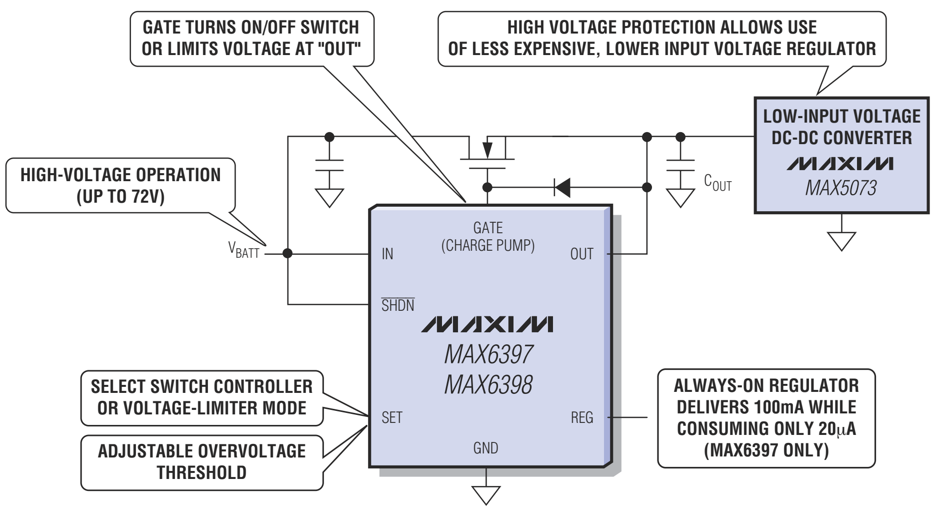


Figure 1 This simple circuit requires only a single IC to balance the charges on two series-connected, low-voltage, high-value capacitors and maintain their common junction at one-half of the supply voltage.

FIRST INTEGRATED, 72V OVERVOLTAGE PROTECTORS IDEAL FOR AUTOMOTIVE APPLICATIONS





Part	Configuration	Unique Features	Temp Range (°C)	Package
MAX6397	Controller/limiter	Always-on regulator	-40 to +125	8-TDFN (3mm x 3mm)
MAX6398	Controller/limiter	—	-40 to +125	6-TDFN (3mm x 3mm)
MAX6399	Controller	UV monitoring, POK indicator	-40 to +125	8-TDFN (3mm x 3mm)

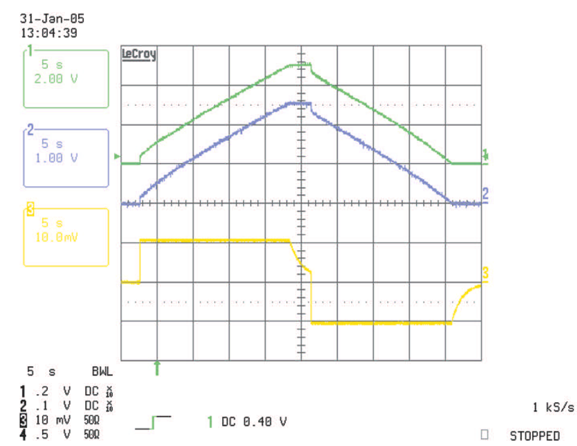


Figure 2 The oscilloscope waveforms within the active-balance circuit show the power-supply rail voltage (top trace), the midpoint voltage at the junction between the two capacitors (middle trace), and the charge/discharge current (lower trace, scaled to 1A per division). The traces reflect a 1A charge interval to 5V, followed by a 1A discharge to 0V. The waveform steps at the start of the charge and discharge intervals are due to the capacitor's internal ESRs.

identical, and the loop equation, including the supply voltage, becomes: $V_{SUPPLY}=V_{C1}(0)+V_{C2}(0)+(C_1\times C_2)/(C_1+C_2)\times\int I(t)dt$. During charging to a 5V-supply level, differences in tolerances between C_1 and C_2 or residual voltages on either capacitor cause the voltage across one capacitor's terminals to exceed 2.5V and cause the other to fall below 2.5V.

To overcome this undesirable mismatch, the LP2996 DDR termination regulator, IC_1, sinks or sources current from both capacitors and actively maintains their voltages at one-half of the supply voltage (**Figure 1**). The LP-2996 provides an active termination for DDR-SDRAM devices and can sink or source large amounts of current; its data sheet's nomenclature and labels reflect its intended memory-support role. The LP2996's Class B output, V_{TT}, drives the capacitors' common connection, actively maintaining the junction at $V_{DDQ}/2$ and becoming active only when the capacitors get out of balance. At balance, the LP2996 wastes no charging current and thus operates efficiently. The device's data sheet specifies that the LP2996's out-of-balance error amounts to a V_{TT} offset of ±20 mV around the $V_{DDQ}/2$ setpoint. **Figure 2** shows charge and discharge waveforms for 1A current steps.

This active balancing circuit does impose some limitations. Using a power supply rated at 5V and 1A, the two capacitors achieve charge balance in a maximum of 25 sec: Charge time=5F×5V/1A. The initial charging interval overcomes any initial prebias charge on either C_1 or C_2. The steady-state current flow into and out of the LP2996 amounts to a fraction of the high current flowing through the capacitors and is just sufficient to overcome any tolerance mismatch in the two. The LP2996 includes thermal-shutdown protection, but an instantaneous short circuit across either capacitor may occur too quickly to activate the protection circuitry.

Thermal considerations determine the capacitor's maximum current-handling capability, and the PC10's data sheet derates the current downward from 2.5A. You can connect 1Ω current-limiting resistors in series with both capacitors if the power supply provides charging current in excess of 2A.

Upon interruption of the power supplied to the circuit, the LP2996 imposes a self-discharge current of less than 1 mA, which represents a capacitor-"battery" discharge rate of 5000 sec per volt into an open circuit. You can reduce the LP2996's self-discharge current by applying an external control signal to its shutdown input. Upon power interruption, the two-capacitor string can supply a constant-current load of 1A for 15 sec over a voltage change from 5 to 2V. You can connect additional pairs of capacitors in parallel to provide additional current, but, depending on capacitance mismatches, initial bias voltages, and current demand, you may need additional LP2996s to maintain charge balance. EDN

Voltage reference is software-programmable

Reza Moghimi, Analog Devices, San Jose, CA

For a variety of reasons, designers often discover that their creations need yet more power-supply voltages. For example, a system powered by ±2.5V power supplies suddenly needs a precision −1.4V reference for a signal-level-shifting circuit and needs a 2.1V reference to drive an ADC. Your options include adding a couple of operational amplifiers and resistors to level-shift and buffer the system's voltage reference or adding a couple of DACs. Op-amp circuits lack programmability to accommodate design changes, and, although the DACs offer programmability, their settings are volatile, and the outputs are typically unipolar and lacking in drive capability.

The circuit in **Figure 1** offers an easy way to generate extra reference voltages and provides a few additional benefits. It allows you to easily generate positive or negative buffered references under software control. Its output buffer sinks and sources as much as 10 mA. You can read and adjust programmed voltages. On-chip storage restores the reference

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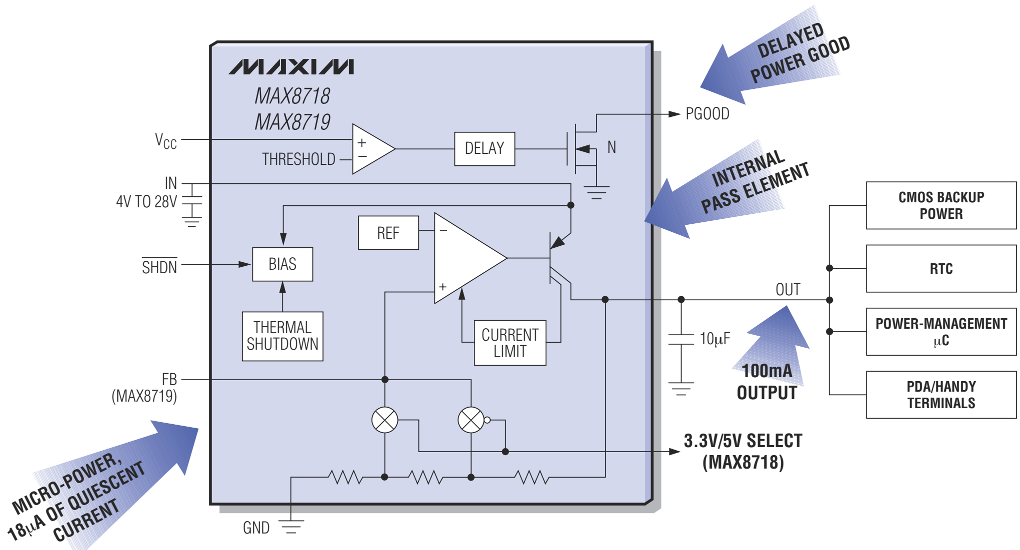
The MAX8718/MAX8719 micropower, linear regulators are ideal for providing always-on, keep-alive power to CMOS RAM, real-time clocks (RTCs), and microcontrollers in systems with high-voltage batteries. Available in small, 3mm x 3mm TDFN packages, the MAX8718/MAX8719 accept input voltages up to 28V, and can power 3.3V or 5V loads up to 100mA with only 18µA of quiescent current. No additional pass elements or dropping resistors are required. For preset output voltages of 3.3V or 5V, use the MAX8718. For adjustable output voltages from 1.24V to 28V, choose the MAX8719.



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- Delayed Power Good Output
- ±2% Output Accuracy
- 100mA Output Current
- 3.3V or 5V, Pin-Selectable Output (MAX8718)
- 1.24V to 28V Adjustable Output (MAX8719)
- Thermally Enhanced 8-Pin, TDFN Package

Part	Output Voltage (V)	Output Current (mA)	Temperature Range (°C)	Package (mm x mm)
NEW MAX8718ETA	3.3/5	100	-40 to +85	8-TDFN, (3 x 3)
NEW MAX8719ETA	Adjustable	100	-40 to +85	8-TDFN, (3 x 3)
MAX1615	3.3/5	30	-40 to +85	5-SOT23
MAX1616	Adjustable	30	-40 to +85	5-SOT23

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voltages after a power interruption, and a parity bit can indicate a malfunction if an internal device failure accidentally causes the programmed voltage to change.

The programmable voltage reference comprises IC_1, an Analog Devices AD8555 high-precision auto-zero instrumentation amplifier, which contains an 8-bit DAC as part of its offset-adjustment circuit. In a change from its intended role, the monotonic DAC generates the output voltage, which can swing from V_{SS} (input code 0) to $V_{DD}-1$ LSB (input code 255). The DAC's 8-bit resolution provides voltage steps of 0.39% of the difference between V_{DD} and V_{SS}—for example, steps of 19.5 mV with a 5V supply. The output-voltage, V_{DAC}, temperature coefficient is less than 15 ppm/°C.

The following equation describes the DAC's approximate internal reference voltage, V_{DAC}:

$$V_{DAC} \approx \left(\frac{CODE+0.5}{256}\right)(V_{DD}-V_{SS})+V_{SS},$$

and the following equation yields the circuit's output voltage, V_{OUT}: $V_{OUT}=GAIN(V_{POS}-V_{NEG})+V_{DAC}$, in which GAIN represents the circuit's default internal gain of 70 for the differential input. Both inputs connect to ground, and the first term is thus close to 0V, or 10 μV maximum due to input-amplifier errors, and the circuit's output voltage, V_{OUT}, is equal to V_{DAC}.

Until you permanently program the internal registers, they allow you to alter the output voltage and explore the circuit's behavior as a fixed-voltage reference and reprogrammable 8-bit DAC. To program the output voltage, you apply the appropriate pattern according to the first equation and instructions from the device's data sheet. After verification, you can permanently set the output voltage by blowing certain of the device's internal polysilicon-fuse resistors. As **Figure 2** shows, for a given output-voltage level, the device's absolute error is less than 0.4% across a −40 to +140°C temperature range. **EDN**

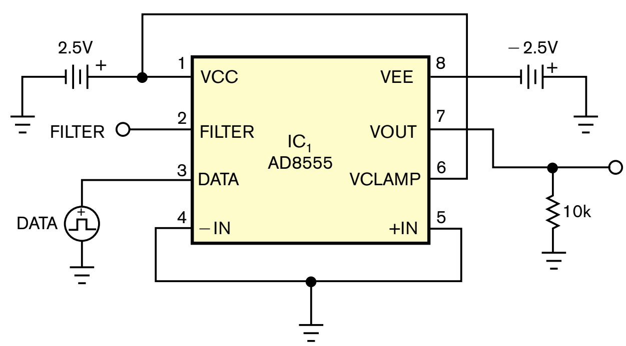
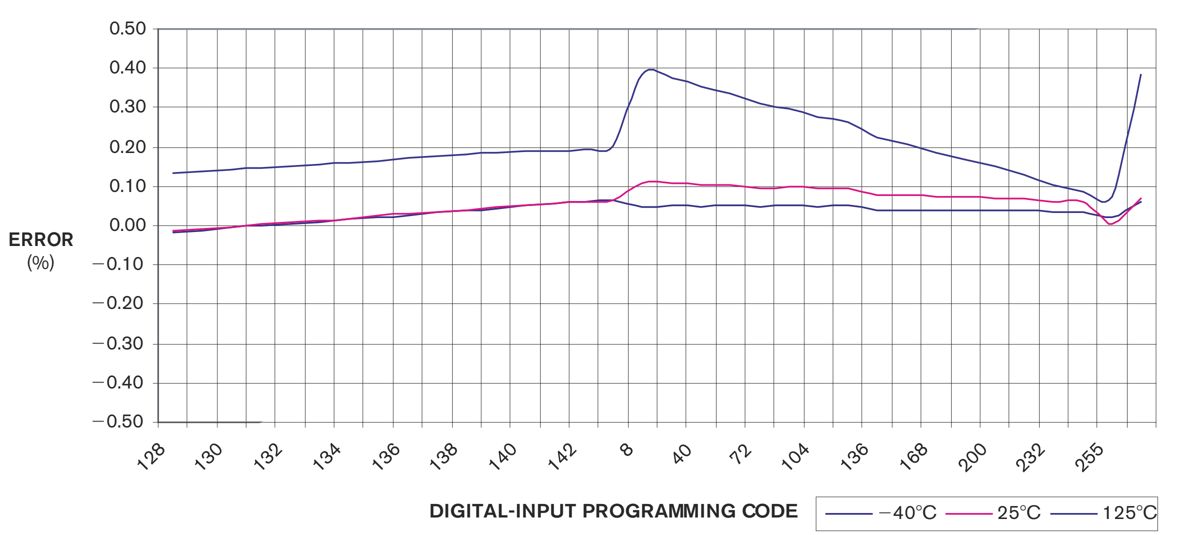


Figure 1 Occupying a tiny, eight-lead LFCSP footprint, a programmable instrumentation amplifier doubles as a last-minute adjustable-voltage bipolar-reference source.



NOTE: PERCENTAGE ERROR=$100\times\frac{V_{OUT(ACTUAL)}-V_{OUT(CALCULATED)}}{5V\ FULL\text{-}SCALE}$.

Figure 2 Output-voltage error for the reference circuit reaches a maximum of 0.4% at a temperature of −40°C and a 5V power supply.

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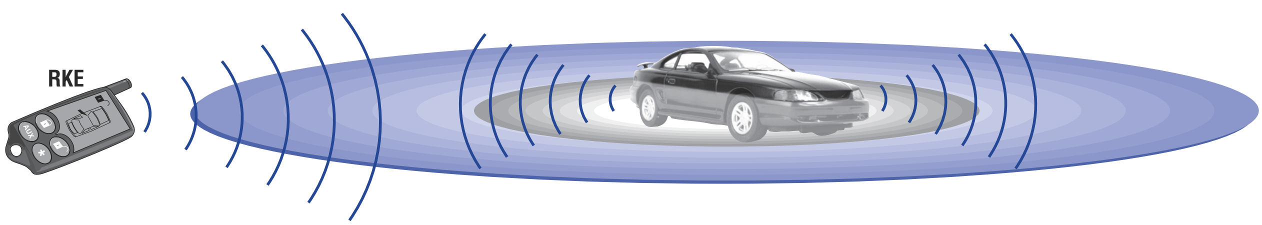

- **+10dBm Output Power**
- **12mA Tx Current (FSK)**
- **-114dBm (ASK)/-110dBm (FSK) Rx Sensitivity**
- **6.1mA Rx Current**

Part	RF Frequency (MHz)	Modulation	FSK Deviation (KHz)
MAX7030LATJ	315	ASK	N/A
MAX7030MATJ	345	ASK	N/A
MAX7030HATJ	433.92	ASK	N/A
MAX7031LATJ	308	FSK	±51.4
MAX7031MATJ15	315	FSK	±15.5
MAX7031MATJ50	315	FSK	±49.5
MAX7031HATJ17	433.92	FSK	±17.2
MAX7031HATJ51	433.92	FSK	±51.7
MAX7032	SPI™ programmable	ASK/FSK	SPI programmable

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productroundup

SWITCHES AND RELAYS

Sealed tactile switches come in a variety of sizes

Available in 3.5×6-, 3.5×7-, and 3.5×12-mm versions, Alcoswitch sealed tactile switches come in through-hole and SMT arrangements. Standard life for the switches is 1 million cycles; however, some parts in the line carry 50,000-cycle ratings. Contact ratings are 50 mA at 12V dc, and all switches carry an IP67 environmental-sealing rating. Versions with location posts for easier product placement are available. Packaging options include bulk, tape, and reel. Sealed tactile switches range from 29.6 to 43.8 cents (10,000).

Tyco Electronics, www.tycoelectronics.com

Switch series features RGB technology

The IS series SmartSwitch uses high-quality red, green, and blue LEDs for color matching, enabling designers to customize control panels with project-specific colors, including RGB white. The STN (supertwist-nematic) SmartDisplay module is available as an LCD with a high-contrast viewing area measuring 13.9×10.6 mm with a 36×24-pixel resolution. The display targets compact electronic devices requiring graphics, text, or moving-image displays in tight locations.

NKK Switches, www.nkkswitches.com

Illuminated emergency-stop switch has a variable supply of voltage

UL-approved, meeting IP65 oil and water standards, and conforming to a variety of EN ratings, the Series 84 emergency-stop switch has gold-plated silver contacts for switch capacity in accordance with EN 60947-5-1. LED illuminations allow a 50,000-operation life span, and a slightly domed actuator head provides visible illumination from a side view. A color ring on the actuator body of the switch allows engineers to see the switch's actuated position. With supply-voltage ranges of 5 to 30V dc, the Series 84 costs $20 per unit.

EAO, www.eaoswitch.com

Solid-state relay has built-in current-limiting circuitry

Current limiting and normally open, the CPC1510 1-Form-A optically isolated SSR (solid-state relay) replaces electromechanical devices and enhances wire-line-interface-application performance. Manufactured in dielectrically isolated silicon technology, the device integrates active current-limit-protection circuitry with the output MOSFET relay switches, providing a thermal-shutdown feature in the relay, allowing power-cross immunity suiting harsh environments. Peripherals include a 250V output-load voltage, 200-mA maximum continuous-load current-handling capability, 15Ω maximum on-resistance for bidirectional applications, and 3.75Ω for unidirectional applications. The CPC1510 OptoMOS SSR costs $1.48 (10,000).

Clare Inc, www.clare.com

Timers come in puck-style package

ST1D Series puck-style-packaged delay-on-make timers include solid-state CMOS digital circuitry, a standard 3A continuous current, an available 10A load current, and one Form A adjustable switching device using a 10-position DIP switch encoded in binary format. Two timing ranges include 0.2 to 102.3 sec in 0.1-sec increments and 1 to 1023 sec in 1-sec increments. Both feature a timing accuracy of

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Intersil High Performance Analog

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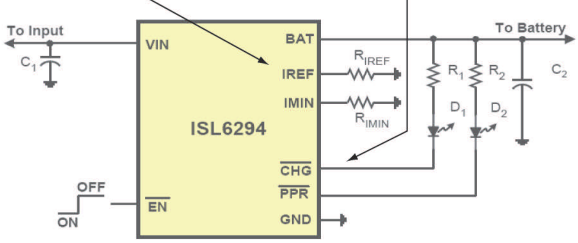
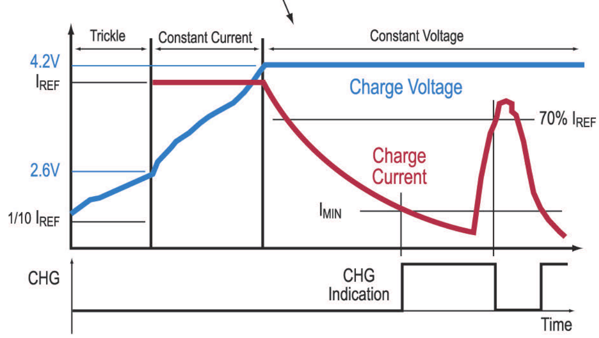
Not only is the 2mm x 3mm ISL6294 the industry's smallest, but this fully integrated, single-cell Li-Ion / Li-Polymer battery charger IC can handle input voltages up to 28V, eliminating the need for an over-voltage protection circuit.

The constant current I_{REF} is set with the external resistor R_{IREF}. The constant voltage is fixed at 4.2V.

End-of-charge (EOC) current indicated through the CHG pin (which can be interfaced to a micro processor), but the charger continues to output the 4.2V.



If the battery voltage is below 2.6V the ISL6294 charges the battery with a trickle current of one-tenth of I_{REF}. When the battery voltage reaches 4.2V, the charger enters a CV mode and regulates to fully charge battery without the risk of over charge.



TYPICAL CHARGE PROFILE

Key Features:

- 2mm x 3mm 8 Ld DFN package
- 28V maximum input voltage
- Programmable end-of-charge current with status interfaced to a micro device through CHG pin
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- No external blocking diode required
- Integrated pass element and current sensor
- 1% voltage accuracy
- Trickle charge for fully discharged batteries
- Less than 1µA leakage current off the battery when no input power attached or charger disabled
- Input over-voltage protection
- End-of-charge indication with large hysteresis to prevent unwanted re-charge

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SWITCHES AND RELAYS

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Amperite Co, www.amperite.com

Pushbutton switch features double-break contacts

Momentary-pushbutton-switch Series 1200 comes in NO and NC models, which can handle 8A at 125V ac and 4A at 250V ac or 24V dc. Featuring butt-action contacts with double break, the switches provide 10,000 cycles of life in a temperature range of −20 to +55°C. All models are bushing-mounted for installation in a 0.480-in. mounting hole and include a 0.315-in.-diameter, dome-topped actuator in black, white, green, or red. A chrome-plated brass actuator with a chrome-plated brass cap nut is also available. Terminations include screw type, screw and clamp, or solder lug/quick connect. Models are available in UL and CSA approvals and cost 79 cents (1000).

APEM Components Inc, www.apem.com

Ultraminiature attenuator relays have range of fixed increments

Ultraminiature Series A150 attenuator relays suiting attenuating RF signals in 50Ω systems over a dc to 3-GHz frequency range eliminate the need for additional external resistors. These single-section, switchable devices feature internal matched thin-film attenuator pads in L, T, or Pi configurations where applicable. Relays come in fixed increments of 1, 2, 3, 4, 5, 6, 8, 10, 16, and 20 dB, so designers can use them individually or in combination to achieve desired attenuation levels. Available in a hermetic canister measuring 12.45×9.53×7.11 mm with a minimum 17.78-mm lead, the A150 costs $62.50 (500).

Teledyne Relays, www.teledynerelays.com

Rugged switches feature shockproof design

The maintenance-free detent-action military rotary multipole and selector switches have double-sided, double-wiping, self-cleaning, spring-wiper blades that close on both sides, providing a shockproof and bounceproof design. Standard models include 25 sections, 75 poles, and 16 positions. With fully enclosed decks, glass alkyd moldings provide insulated compartments that separate compartments and achieve a positive index with a specially designed star wheel that uses four spring-loaded ball bearings. The spring-return models use coil springs. The detent-action military switches cost $185.

Electroswitch, www.electroswitch.com

Slide switch saves board space by replacing jumper pins

Allowing compact surface-mount switches to replace conventional jumper-pin-and-wire arrangements, the CAS series of slide switches comes in DPDT and dual-SPDT configurations; the SPDT device measures 5.4×2.5×2.5 mm. Twin gold-plated contacts provide stability and a contact resistance of less than 50 mΩ with gull-wing or J-hook terminations. The switches have an operating-temperature range of −40 to +85°C. The SPDT CAS switch costs 61 cents (1000).

Copal Electronics Inc, www.copal-electronics.com

RoHS-compliant miniature relay handles 1000W lamp load

Weighing 10g, the WJ106 Series relay comes with SPST NO, SPST NC, or SPDT contact arrangements. These contact arrangements are 20A at 125V ac, 16A at 277V ac, TV-8 at 125V ac, 1-hp 125/250 NO, and 0.5-hp 125/250 NC with a maximum switching power of 420W and a 4500 VA maximum switch voltage of 380V ac or 110V dc. WJ106 relays have a life span of 10 million cycles and cost 47 cents (10,000).

CIT Relay & Switch, www.citrelay.com

Lighted pushbutton switch provides four switch/circuit operations

Dual and quad lighted displays are available in a range of SPST- to DPDT-switch functions in the 644-2100 series units. Designers can use one unit in place of four switches, reducing panel-mounting requirements by 75%. This approach allows installation from the front of the panel, attachment through a mounting sleeve retaining the switch housing, and the ability to fit into a standard 0.698-in.-sq hole. Accepting both 3-mm, T-3, submidget, flange-based lamps and LEDs, the device allows front replacement of the light sources. Switch action comes in momentary, momentary snap-feel, or alternate action. Peripherals include 2A resistive, 0.5A inductive, and independent lamp circuits, costing $159 (100 to 249).

Electro-Mech Components, www.electromechcomp.com

EDAs

IC-prototyping tool adds multimode, multicorner support

The Pinnacle IC-prototyping tool now supports multimode, multicorner synthesis and placement. Additions to the tool include a detailed native-analysis kernel, a sign-off-quality timing-analysis engine enabling data tool sharing between floorplanning and synthesis engines, and an adaptive-variability engine that allows users to monitor modes and variability throughout the flow. A one-year license for the IC-prototyping tool costs $395,000.

Sierra Design Automation, www.sierra-da.com

Upgrade for FPGA-tool suite supports SDC format

Version 6.2 of the Libero FPGA-design suite adds support for the Synopsys design-constraint-timing format, an IBIS (I/O-buffer-information-specification)-model generator, and a vendor-specific version of Mentor Graphics' ModelSim simulator. The IBIS-model generator adds RLC data for the package type and pins and assigns appropriate pin numbers, signal names, and I/O-model names. The Windows version costs $2495, and the Unix/Linux version costs $4995.

Actel, www.actel.com

API provides fivefold circuit-simulation-speed increase

Providing a five-times speed increase over its predecessor, the MSIM API omits the use of I/O files and combines application-software modules with the MSIM engine, creating a single executable program. The module and engine combination allows third-party tools to quickly access the simulation engine, producing faster results from the engine. Perpetual-license support for models including BSIM3, BSIM4, and SOI costs $15,000.

Legend Design Technology, www.legenddesign.com

EMBEDDED SYSTEMS

PCI-bus GPID card handles high-volume data transfers

The 32-bit, 33-MHz, PCI-bus-compatible PCI-3488 controller card provides an interface between GPIB instruments and PCI-equipped systems compliant with IEEE4488.1 and IEEE488.2 standards. The interface supports 3.3 and 5V PCI environments, features a 1-kbyte onboard FIFO, and provides an onboard CPLD with a 1.5-Mbps maximum data-transfer rate. The PCI-3488 costs $240 at an introductory rate until Aug 31, 2005.

Adlink Technology Inc, www.adlink-tech.com

AdvancedTCA chassis suits ETSI applications

A 16-slot, full-mesh backplane and thermal stimulation allow superior front-to-rear cooling for the 13U AdvancedTCA chassis, available in the 23-in. size and suiting ETSI (European Telecommunications Standards Institute) applications. Peripherals include dual redundant shelf managers, which designers can plug into the card cage without using any of the 16 slots; 13U height; dual fan trays with four 150-cfm fans below the card cage; and one fan tray above the card cage. All fans have PWM input/tachometer-output capability and have removable air filters. The 13U ATCA chassis costs $5000.

Elma Electronics, www.elma.com

CPU targeting PC/104 systems includes six serial ports

The model 303 CPU includes six serial ports; two serial ports are fully featured RS-232s, and the other four are three-wire ports. The device also includes two USB 2.0 channels and a 1000BaseT Ethernet port for rapid communication. The product's low-power Elan SC520 runs at 133 MHz, is x86-code-compatible, and comes with 32 Mbytes of soldered-on flash memory, a Compact-flash-memory card, and sockets for 128-Mbyte SDRAM. The BIOS is programmed into the onboard flash, suiting portable-system applications and operating systems using the Compact-flash module. Hard-drive storage is available through the IDE port. Single pieces cost $674 and $471 (100 or more).

Sensoray, www.sensoray.com

Two-slot ATCA backplane suits prototyping

With point-to-point mesh topology that requires no switch cards, the two-slot ATCA (AdvancedTCA) backplane features a 10-layer stripline design for routing through signal-integrity studies. The product also includes connectors for direct plugging of the IPM sentry shelf manager or wired connections to other shelf managers. The ATCA costs $700 and has an optional full mesh implemented on the backplane.

Elma Bustronic, www.elmabustronic.com

Still-image class driver provides PTP support over USB

Providing USB support for the Nucleus RTOS, the still-image class driver uses the USB interface and

PTP (Picture Transfer Protocol), enabling designers to use embedded products with USB- and PTP-compliant imaging devices. Licenses for Nucleus USB software cost $14,995, and licenses for the class drivers cost $2995, including source code and without royalty fees.
Accelerated Technology, www.acceleratedtechnology.com

Lynx board has low power draw

With a power draw of less than 5W, the PC/104-Plus Lynx board comes with the x86-compatible, 486-class AMD Elan SC520 processor. Onboard features include 64 Mbytes of soldered-on SDRAM, four communications ports, Ethernet, an IDE, an LPT, a floppy interface, keyboard/mouse ports, and support for ISA and PCI add-on modules. The board includes OEM-enhanced, field-upgradable, customizable BIOS and suits embedded operating systems, including Windows CE, Linux, VxWorks, QNX, DOS, and other real-time OSs. The Lynx costs $399.
VersaLogic Corp, www.versalogic.com

Secure wireless access for networked embedded devices

Including optimized versions of Wind River's VxWorks and Embedded Linux, the ASAP (air-secure access point) complies with the WiFi 802.11 protocol, networking, management, and security-software components. This wireless software converts tethered embedded devices into untethered embedded devices accepting connections from wireless clients. The software supports all necessary protocols in a framework connecting generations of security from WEP (wired-equivalent private) through WPA (wireless-protected access) to WPA2/802.11i in personal (pre-shared-key) or enterprise (802.1X) mode. The ASAP's price ranges from $15,000 to $50,000, based on the number of components.
Embedded Components, www.embeddedcomponents.com

Card adds storage feature

Increased connectivity for the dual 1-GHz PowerNode3 computing node is featured in the ultrawide SCSI PMC (PCI mezzanine card). Peripherals include 512 Mbytes of memory, 3264 Mbytes of flash, front and rear P0 connection, and throughput as high as 40 Mbps. The PowerNode3 comprises dual and single Motorola PowerPC G4 7457 processors running at 1 GHz, each with 2 Mbytes of L3 cache and 2 Mbytes of private SRAM linked through a 133-MHz Avignon host bridge. The device can access as much as 1 Gbyte of onboard SDRAM at bus speeds of 133 MHz, and the board provides 64-bit, 66-MHz and 32-bit, 33/43-MHz PCI slots. The PowerNode3 SCSI PMC bundle costs $7910 (one).
Thales, www.thalescomputers.com

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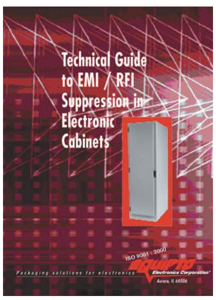
Free Tech Guide For EMI/RFI Suppression



Metals compatibility, performance tests, performance concerns, and real world practicality are just some of the subjects in Equipto Electronics new, free, "Tech Guide For EMI/RFI Suppression." Well illustrated with photos, charts and graphs, the Guide covers what's important along with the concerns engineers should contemplate when designing for EMI/RFI suppression in electronic cabinets. Also included are illustrations on seismic hardening and methods of joining multiple bay FCC shielded cabinets.

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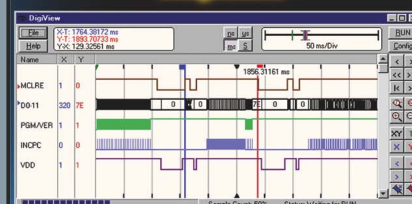

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YESTERDAY'S HYPE MEETS TODAY'S REALITY

STATS 2001: Macintosh only, Firewire signal interface, $400 price tag / 2004: 8 million sold

iPod defines a new way of listening and a new culture

In an industry that craves the next big thing to drive sales, define a market, and even become a cultural phenomenon, Apple's iPod scored a big win by any criterion. The first such device—for Macintosh only—debuted in October 2001. The device, weighing 50g, included a scroll-wheel user interface, an LCD, a 1.8-in. hard drive, and a FireWire signal interface. Despite the relatively high price of $400, the unit and concept quickly caught on: Apple sold 125,000 units by the end of 2001. Apple shipped its millionth iPod by June 2003; at the end of 2004, approximately 8 million units were in users' hands. And an uncountable number of vendors offer accessories, docking systems, auto interfaces, and more.

The iPod also demonstrates the short life cycles of today's consumer products. Just four months after the initial release, Apple released a 10-Gbyte version, along with some bug fixes; in July 2002, it announced a 20-Gbyte version, along with price cuts on the other versions, and PC compatibility. At the end of 2002, a smaller, third-generation iPod with a different button layout and connectivity, along with the iTunes service, emerged. The latest version, the flash-based iPod Shuffle MP3 player has only a USB 2.0 interface, lacks a click wheel and LCD, and sells for just $99.—by Bill Schweber, Executive Editor